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EVALUATION OF TRANSISTORS AND DIODES FOR MICROPOWER CIRCUIT APPLICATIONS

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SUMMARY

Semiconductor devices suitable for use at power levels below 1 milliwatt per stage have been difficult to obtain and are not usually characterized for use at sufficiently low levels of current. This report presents low-level parameters for a number of transistors and diodes as a guide to selection and in adequate detail for most circuit design. The data presented were used to characterize transistors for logical switching circuits; however, the data can be applied equally well to the selection of devices for micropower linear applications. These data should be of use to anyone attempting to design circuitry operating at power levels less than 1 milliwatt per stage.

INTRODUCTION

Man's exploration of space has created a number of new technological requirements of which circuits operating at very low power levels is an important one. Generally, systems designed for space applications are severely limited in size and weight and to a lessening extent by the amount of electrical power available. Microminiaturization has markedly reduced size and weight. Micropower circuits (i.e., circuits operating at power levels of less than 1 mw/stage) can make these advances of practical use by reducing both the power required for large and complex systems and consequently the heat that they must dissipate. Heat is fast becoming a problem with microcircuits capable of packaging densities of one-half million components per cubic foot.

Most of the applications in which micropower circuits can effect considerable improvements involve digital systems for satellites and other space vehicles. Data handling, data processing, and advanced guidance and control systems are all basically special purpose computers, and they can profit greatly from low-power circuitry. In these cases the majority of circuits are digital and are readily built with micropower techniques since the absolute power level at which they operate is of no consequence. The few analog circuits involved can be treated in similar fashion except where they are required to supply output power to another system or device.

Development of suitable micropower circuits for the above applications

has been hampered until recently by the scarcity of suitable semiconductor devices. Even those fully suitable devices were characterized at power levels far too high for micropower use. It was, therefore, necessary to determine the parameters most affecting micropower operation and to screen a number of promising devices on this basis. This report is the result of such a study that was initiated early in 1962 to select transistors and diodes suitable for use in satellite electronics operating at power levels of 1 to 100 microwatts per stage. The circuit design portion in this program has already been reported in reference 1.

Devices included in this report are all silicon or gallium arsenide. All other presently available materials fail to operate satisfactorily over the wide temperature range required by the space environment. Initially, transistors were screened on the basis of high current transfer ratio, low leakage current, and high alpha cutoff frequency. As the latter parameter is normally specified at currents in the milliampere region, it turned out to be a poor measure of the capability of the device at microampere levels. From preliminary data obtained on a number of devices, tentative specifications were submitted to several manufacturers and selected devices obtained. In all cases these transistors had considerably higher gain at low collector currents than the similar transistor specified for normal current operation.

In addition to determining their low-level parameters, some of the more promising transistors were subjected to temperature cycling and high-temperature storage tests. The intent of these tests was to determine the relative merits of the transistor rather than to make any accurate prediction of their absolute failure rate. In all cases these tests were conducted with no voltages applied to the devices.

Obtaining diodes suitable for micropower use was not as difficult as obtaining suitable transistors; therefore, efforts were limited to room-temperature evaluation of available diodes primarily for leakage, junction capacitance, and forward voltage.

The data contained in this report are essentially necessary for the design of logic circuitry. The significant difference between them and the usual published data is that these data have been taken at low values of current ranging from 1 to 1000 microamperes, whereas most published data are given in the milliampere region. In addition, data on the required speedup capacitor for switching circuits and on the junction capacitances have been included since they become particularly important at low power levels. A limited amount of accelerated life test and temperature cycling data has also been included.

CHARACTERISTICS OF TRANSISTORS FOR MICROPOWER APPLICATIONS

The purpose of this section is to identify the transistor parameters most important to micropower operation and their effects on circuit operation. Further information on transistor and diode parameters as well as a discussion of typical micropower circuits can be found in reference 1.

Both minimum power and speed of operation are ultimately limited by the

characteristics of the active devices used in a circuit. This limiting effect starts to manifest itself at power levels below approximately 1 milliwatt per stage. The parameters most limiting circuit performance are current gain and leakage current for power, and junction capacitance and storage effects for operating speed.

The ultimate use of the transistors selected was digital circuitry for satellite logic applications. Most of the circuitry was of the complementary symmetry type, which helped to relax some of the specifications; however, the best of the available devices were sufficiently good for even more critical applications. The maximum desired operating rate of these circuits was approximately 10 kilocycles, which turns out to be reasonable for circuits dissipating 10 to 100 microwatts per stage.

Direct-Current Limitations

Transistor parameters are basically current dependent and are little affected by operating voltage so long as it exceeds 1 or 2 volts. The obvious first step in reducing circuit power consumption is to reduce the supply voltage to the lowest possible value. Further power reduction must then be obtained by reducing the operating current. The amount that the current can be decreased is limited by two basic characteristics of the transistor - current gain and leakage current.

Direct-current gain H_{FE} of a transistor is strongly influenced by the collector current at which it is operated. For typical low-power transistors the current gain reaches a maximum at 1 to 10 milliamperes collector current and falls off at both larger and smaller currents. This characteristic is much less pronounced in planar transistors, thus making them much more desirable for micropower circuits than most other types.

Planar transistors currently available have current gains greater than 10 at collector currents of less than 0.1 microampere. This gain is sufficient for the design of many types of logic circuits and permits extremely low-power operation where operating speed is low.

Operation at such low currents magnifies the problems normally encountered with leakage currents. It is necessary to select transistors that will have leakage currents small with respect to the operating current under simultaneously worst-case conditions of component tolerances and at the highest temperature of operation. Passivated planar transistors are again good in this respect. By the elimination of surface effects in their construction, the leakages are in many cases reduced close to the theoretical minimum imposed by thermal carrier generation within the junctions. Leakage currents actually measured are, in the case of some of the best transistors, in the range of tens of picoamperes (10^{-12} amp). This figure is sufficiently low so that even allowing for an increase of 100 in the leakage current with a rise of operating temperature results in a leakage that is small compared to any reasonable operating point; namely, 1-microampere collector current.

In addition to the previous requirements, a low base-emitter voltage V_{BE}

as well as a small temperature coefficient of V_{BE} and a low collector saturation voltage $V_{CE(sat)}$ are desirable for circuits to be operated at minimum voltage levels. If supply voltages of 5 volts or more are used, the V_{BE} requirements become much less critical and have a corresponding smaller effect on circuit performance.

Switching-Speed Limitations

Contrary to the factors limiting speed at normal power levels, the alpha cutoff frequency given by the manufacturer is usally a poor measure of transistor performance at micropower levels. At collector currents below approximately 100 microamperes, the switching speed of circuits using resistors as the direct-current collector load become limited primarily by R-C time constants.

Any stray capacitance from collector to base will also be magnified, because of the Miller effect, so that for maximum speed operation this capacitance should also be minimized. One way to accomplish this is to use a transistor electrically isolated from its case and ground the case. Complementary circuits are superior to conventional circuits utilizing collector load resistors, since replacing the collector resistor with an active device lowers the effective output impedance, and therefore the R-C time constant, to very low levels. Complementary circuits cannot solve all time-constant problems, however, because a similar effect takes place at the input of the circuit.

When it is desired to compute rise and fall times of micropower circuits it can be done with reasonable accuracy by using the hybrid π equivalent circuit and by taking into consideration all junction and stray capacitances. Some simplification of calculations can be achieved by considering the transistor as a charge-controlled device (refs. 2 and 3). Applying this concept, the charge necessary to turn a particular transistor on for various collector currents can be determined; this is actually the charge necessary to raise the transistor equivalent input capacitance to the conduction level.

This charge is of particular interest in that it directly determines the value of speedup capacitor necessary in a digital circuit. It is this speedup capacitor, in conjunction with the base resistor that it shunts, that forms an R-C time constant, which ultimately limits the operating rate of the stage. The speedup capacitor, and, therefore, the turn-on charge required, is a function not only of collector current but also of the turn-off bias voltage. For rapid turn-on and highest operating rate one should use the minimum turn-off bias voltage. When only turn-on effects are considered, silicon transistors can in many cases be operated with zero turn-off bias.

Rise times can be kept quite short, that is, less than 1 microsecond, even in circuits operating at collector currents of a few microamperes. This is true since it is possible to turn on rapidly a lightly loaded transistor. Fall times, on the other hand, are dependent on the R-C time constants previously discussed. A further detrimental effect is experienced because of minority carrier storage within the junction. These carriers maintain current flow

after the input current has been removed until such time that they are swept out of the junction area or recombine. Connecting the base-return resistor to a supply providing reverse bias will speed up the process but not without some penalties in drive requirements. As in normal power circuits, the amount of overdrive used also affects storage times markedly.

EVALUATION OF SILICON TRANSISTORS FOR MICROPOWER APPLICATIONS

Summarizing the previous section leads to the criteria for selecting a transistor for a particular micropower application. Actual values of the parameters will be used as an example. In this specific case operation at collector currents of approximately 10 microamperes was desired with a single supply voltage of 4.5 volts. The operating rate was to be in the range of 10 to 100 kilocycles, and temperature extremes of -20° to 80° C were expected.

(1) The forward current transfer ratio H_{fe} should be as high as possible at the selected operating point and over the expected temperature range. A minimum H_{FE} of 40 at room temperature was chosen as sufficient.

(2) The collector-base leakage current I_{CBO} under worst-case operating conditions should be at least a factor of 10 below operating current. High limit I_{CBO} of 10 nanoamperes at room temperature is reasonable.

(3) The base-emitter voltage V_{BE} should be low and uniform. With a supply voltage of 4.5 volts and resistor capacitor transistor logic (RCTL), this parameter is not critical. With other logic forms, such as direct coupled logic or supply voltages of the order of 1 volt, it would be necessary to insure a small spread in the values of V_{BE}. A low-temperature coefficient of V_{BE} would then also be desirable.

(4) Input and output capacitances should be a minimum. In both cases values of approximately 10 picofarads are practical.

(5) The storage time should be a minimum. No quantitative data were taken on this parameter directly; however, transistors were compared for their effects in typical circuits.

(6) Low turn-on charge is also important.

By taking into account the basic parameters of interest, a number of transistors were selected from manufacturers' specifications and recommendations, and their low-level parameters were measured. The results comprise tables I and II. Of the transistors available at the time, the Fairchild S-4528 and S-4529 were selected as representing the best compromise of all parameters in an approximately complementary pair. These two transistors are selected for micropower use from the families that include the 2N995 and 2N996, and the 2N915, respectively. Larger samples of the S-4528 and S-4529 transistors were then obtained and subjected to high-temperature tests, the methods and results of which will be discussed in the next section. Two transistors are included in tables I and II that have been released since the original selection was made. These are the 2N2432 and 2N2412. They both show promise for low-power

operation and were included for that reason.

Detailed parameters of the S-4528 and S-4529 are included as tables III and IV and figures 1 to 6 and are believed to be sufficiently accurate and typical for circuit design. Tables III and IV are the purchase specifications for the two transistors selected as the best compromise from among those tested.

Figure 1 shows the variation in required speedup capacitance with collector current for the S-4528 and S-4529 transistors for various off-bias voltages. These data were taken using the conventional common-emitter inverter circuit shown on figure 1(a). The variable capacitor was adjusted to the minimum value that would produce the fastest rise output pulse without overshoot. This value was taken as the speedup capacitance for that particular collector current. Both base and collector currents were varied by selection of the resistors used.

Figure 2 is a typical common-emitter characteristic for the S-4529. It was plotted directly on an x,y-plotter using a carefully shielded test fixture and high-input-impedance amplifiers. It is typical in shape to the characteristics obtained for both the NPN and PNP transistors, the only notable difference between them being the gain (see tables I and II).

Figure 3 indicates what change in leakage currents can be expected with temperature. The actual values were obtained from some of the first transistors purchased and are somewhat lower than the averages shown in tables I and II. Note that they were also measured at lower voltage levels. The trends are nevertheless valid and can be used for design calculations by a shift of the current scale to bring the curves into correspondence with a measured room-temperature leakage.

The capacitance of a semiconductor diode is a definite function of voltage and the two junctions of a transistor are no exception. Figure 4 shows this effect. Capacitance values quoted on manufacturers' data sheets may be measured at different values of junction voltage. These curves allow an easy comparison with other planar devices. They also allow comparison of the capacitance data tabulated in tables I and II (taken at zero bias) with manufacturers' data.

Figure 5 shows the input diode characteristics of the two selected transistor types over a range of temperatures. The range of base currents has been selected to present the most usable data for micropower circuit design. If supply voltages of 1 to 2 volts are to be used, the temperature coefficient of V_{BE} shown in figure 6 becomes important.

Additional characteristic curves for several other devices that show promise for micropower applications are presented in appendix A. Some of these devices became available after S-4528 and S-4529 were selected; therefore, these devices were not investigated in as much detail.

PARAMETER STABILITY OF THE S-4528 and S-4529 TRANSISTORS

Stressing Tests

The relative stability of the parameters was determined by subjecting lots of 20 or more of the transistors to elevated temperature storage and/or temperature cycling schemes. Table V gives the details of the stressing profiles.

Elevated temperature was utilized to accelerate physiochemical reactions and failure mechanisms because of unavoidable imperfections in the transistor structure. These reactions are impurity migration within the crystal structure, adsorption of contaminators adjacent to the crystal structure, impurity diffusion along crystal dislocations, and the like. Imperfections are considered to be such items as incomplete surface passivation of the junctions and poor lead bonding and hermetic seals.

A temperature of 200° C was chosen for storage and as the upper limit for cycling. This temperature was chosen for several reasons. First, the manufacturer of the two transistors apparently best suited to our work (Fairchild) commonly used this temperature in accelerated reliability testing. Secondly, the temperature of 200° C was the most common absolute maximum temperature for semiconductor devices available at the start of this study.

It was desired to use as high a temperature as practical to accelerate testing. Some extrapolation of performance could then be made by using the Arrhenius rule of physical chemistry, which states that the rate of chemical reactions is approximately doubled with each 10° C rise of temperature. Since the expected primary causes of parameter variation would be because of chemical reaction of contaminants, this rule should be applicable.

Cycling between 200° and -55° C was done on a limited basis in order to promote electrical failures, which were due to the mechanical stressing action of cycling. The quality of the bonds of the lead wires to the transistor chip was of prime interest in this portion of the study. The upper limit of temperature was established as outlined, and the lower limit arbitrarily set above the manufacturer's recommended minimum storage temperature of -65° C.

The transistors, which were subjected to the cycling tests, were allowed at least 15 minutes to reach thermal equilibrium at each extreme in temperature and were subjected to a total of 63 cycles. The number of cycles used far exceeded the five cycles specified in references 4 and 5.

The tests reported herein depart markedly from the manufacturer's type of reliability tests where power dissipation tests are necessary to establish mean times to failures and failure modes for units intended for operation in the range of hundreds of milliwatts of dissipation. No attempt was made to test the transistors under power dissipating conditions, since they are intended to be used for logic circuitry, which requires power dissipation in the transistors in the order of 1 to 500 microwatts. Basically, the S-4528 and S-4529 are capable of dissipating a maximum of 360 milliwatts in an ambient of 25° C. (See tables III and IV for further specifications for S-4528 and S-4529). If the transistors were placed on simulated power dissipating condi-

tions, the previous conditions would give power derating ratios roughly within the range of 0.0001 to 0.1 percent. Silicon transistor failure rates as functions of temperature are discussed in reference 6 (see fig. 63 of ref. 6). Extrapolation of the derating ratios down to 0.1 percent ratio and below would show a small change in failure rate with power derating ratio. Since this change would be small, testing was done under zero-power dissipating conditions.

Parameters Checked

The three parameters investigated for stability are the collector-base leakage current I_{CBO}, emitter-base leakage current I_{EBO}, and the common-emitter current gain H_{FE}. Figure 12 in appendix B shows the circuits, conditions, and equipment used to measure these parameters. The voltage levels chosen conform to those acceptable for micropower circuit design.

Discussion of Results of Transistor Stability Evaluation

Table III lists the stressing profiles used and enumerates the catastrophic and degradation failures observed for each lot. Note that the limits set for degradation failures are quite arbitrary. They were set to eliminate transistors showing changes in characteristics that might indicate a tendency to early failure. Nearly all of the transistors listed as degradation failures would operate satisfactorily in most micropower circuits; however, they would be rejected for use in the construction of flight hardware as potential reliability risks.

The first five lots (A to E) were composed of the type S-4529 NPN transistor, which is a selection from the family including the 2N915. At this time the S-4529 was a relatively new device although it did not represent a large improvement in the state of the art. The data presented in tables VI to VIII show the stability of these devices. Collector-base leakage current I_{CBO} increased by less than 16 percent for all the percentiles tabulated, except for lot B - stressed both by cycling and storage - where the increases were as high as 67 percent. Forward current transfer ratio H_{FE} showed only a slight variation, and that being in general an increase. Emitter-base leakage current I_{EBO} was similarly constant with the exception of two transistors in lot B. One of these increased more than 200 percent and was therefore classed as a degradation failure. The other increased substantially but not sufficiently to be classed as a failure. Since the lot size was only 20 units and the data for all transistors were included in determining the percentiles shown, these two transistors caused a 27-percent increase in the 10th percentile value for this lot. The other percentiles for this lot as well as those for all other S-4529 lots exhibited a variation of roughly 25 percent or less.

Lots F and H consisted of S-4528 (PNP) transistors, which are a selection from the family including the 2N995 and 2N996. At the time these devices were purchased, they were quite new and were not yet in full production. The one catastrophic failure in lot H proved under microscopic examination to be a failure of the bond between the gold lead wire and the emitter area of the transistor chip. Correspondence with the manufacturer indicated that the

process of lead wire bonding was being changed to eliminate further failure of this type.

A partial explanation of this catastrophic failure, as well as the numerous degradation failures occurring in lot H may lie in a series of failures of the environmental test equipment. The original plan was to subject this lot to a minimum of 50 temperature cycles, much as the NPN transistors. Unfortunately, the temperature chamber used for the cycling malfunctioned from the start overshooting the -55° C temperature limit and jamming at about -100° C on several of the five cycles. In addition, it also overshot the 200° C temperature at least once, overheating to 260° C or possibly more for an undetermined time. Lot F was not temperature cycled at all; hence, it is difficult to conclude if a possible difference in manufacturing techniques between lots F and H or if the extreme stressing of the abnormal cycling caused the catastrophic failure. Likewise, the greater number of degradation failures of lot H than of lot F cannot be adequately resolved.

As in the case of the S-4529 (NPN) transistor, the parameter percentile data shown in tables VI to VIII for the S-4528 (PNP) transistor include the degradation failures. It is noteworthy that even with this restriction the overall variations in the percentile curves are no worse than those of the NPN groups, except for the I_{CBO} percentiles where the variations were as high as 48 percent.

It is seen from the results listed in table VI that failures, both catastrophic and degradation, have the greatest frequency when the transistors are both temperature cycled and temperature stored. The I_{CBO} degradation failures of lots B and F are the exceptions of the total failures listed. In the lot B case, the failure occurred during temperature storage.

CHARACTERISTICS OF DIODES FOR MICROPOWER APPLICATIONS

Limits on the parameters of micropower diodes are very similar to those of the transistors with which they are used. Leakage, diode capacitance, and forward drop all degrade the circuit performance in much the same manner as the corresponding transistor parameters. Leakage and junction capacitance are the more important parameters. Forward drop becomes a limiting factor for circuits operating at the lower limit of supply voltage, which is in the range of 1 to 3 volts for silicon devices.

Direct-Current Limitations

Diode leakage problems are usually most severe in gating circuits where a number of diodes are connected to a common point. Leakages in this case are cumulative. When the common point is the base of a transistor, the effect of any small current that does flow will be multiplied by the transistor gain.

If low-power stages with high-output impedances are used, diode leakage may couple the various stages with common gates. This problem can be neglected for complementary logic with its inherent low-output impedance.

Less critical of leakage are diodes used for clamping, clipping, or other protective functions. In these cases the diodes are used singly, and so long as their individual leakage is small compared to the current in the associated circuit no difficulty will occur. Actually, each circuit must be evaluated separately for leakage effects, but if the total diode leakage in any circuit meets the previous criteria one is generally safe. This evaluation must, of course, be carried out for worst-case conditions.

It will be shown in a following section that low-capacitance diodes are desirable. If a diode is chosen primarily for this parameter, one would normally select a computer-type diode, a number of which are available with quite low capacitances. The manufacturing process of this type of diode usually includes a doping process that introduces gold or some other impurity to decrease the storage time. This process has the undesirable side effect of increasing the leakage current. A tradeoff must therefore be made between the speed and leakage. In nearly every case this will not prove to be a limiting factor for micropower circuits since there is a similar tradeoff imposed by the transistor that dictates increased power levels, and therefore currents, for higher operating speeds. In addition, planar microdiodes with small geometries, and therefore low capacitance and leakage, are becoming available.

The minimum supply voltage for a logic circuit is determined predominantly by the sum of the voltage drops in the driver stage, coupling device, and input of the following stage, plus the effects of temperature. Diodes used for coupling, as in gating circuits, are therefore required to have a low forward drop if minimum supply voltages are to be used.

If the circuit must operate over a wide temperature range, the temperature coefficient of forward drop also becomes important. Any change in the V_{BE} of the transistor or the forward drop of the diode can be considered as a component tolerance. Increasing the tolerance of any circuit component has been shown to increase the circuit's power consumption (refs. 7 and 8).

Switching-Speed Limitations

Diodes with sufficiently low leakage for use in very low-power circuits will probably not limit circuit performance because of their recovery time, since these circuits are presently limited to low-frequency operation. Diode capacitance may be much more serious. In the case of both diode gates and diodes used to prevent high reverse voltages across a transistor base-emitter junction, the diode capacitance adds directly to that of the transistor. This has the effect of increasing the turn-on charge requirements of the transistor and thus decreasing the maximum repetition rates attainable.

A second detrimental effect of large diode capacitance is the possibility of false triggering by signals that would have been blocked by an ideal diode. This would be of particular importance for circuits having fast rise and fall times; the high-frequency components could readily be passed by a small capacitance.

EVALUATION OF DIODES FOR MICROPOWER APPLICATION

Summarizing the previous section leads to the following criteria for the selection of diodes for micropower applications: (1) Diode leakage should be low in comparison to the minimum current flow in the circuit at maximum temperatures, and (2) where several diodes are used together the sum of leakage currents must meet this criteria.

Diode capacitance should be as low as practical. In clamping and protective applications, where leakage is not quite as important, the diode selection should be for *minimum* capacitance.

A number of low-leakage diodes as well as some readily available diodes were tested and compared for leakage, forward drop at low currents, temperature coefficient of forward drop, and junction capacitance. The results are presented in table VI in order of increasing leakage. A tabulation of spread of forward drop is included as a rough estimate of the degree of control of the manufacturing process. In as much as this variation must be considered in circuit design, it might be necessary to select diodes to a tight tolerance forward drop for critical applications.

Another factor that must be considered is the variation of forward drop with current. Table IX also shows the temperature coefficient of several diodes and their variation with current. They all show an undesirable increase in temperature coefficient at decreasing currents.

One of the most interesting facts revealed by this investigation is the low-temperature coefficient exhibited by the gallium arsenide diode tested (fig. 7). Its forward drop is comparable to that of similar silicon units, yet its temperature coefficient is notably less. A design study evaluating minimum supply voltages as a function of diode parameters indicated as much as a 25-percent saving in supply voltage using a gallium arsenide diode over a temperature range of 100° C. The particular diodes tested are no longer manufactured, but Texas Instruments may market a comparable device in the near future.

DISCUSSION OF RESULTS OF DIODE EVALUATION

Diodes with sufficiently low leakage for micropower circuits operating with base currents of a micorampere or more are readily selected from the better low-speed planar diodes. Several of these had leakages of less than 1 nanoampere. Their capacitances are approximately 5 picofarads at zero voltage, which is reasonable, but they could be better. The best of the microdiodes had leakages an order of magnitude larger, but exhibited capacitances of 1 to 2 picofarads. They would therefore be more desirable as clamping or limiting devices. For all but the lowest power circuits they approach the ideal except for poor matching of forward drop.

With the continuing trend to microminiaturization there is an increasing number of microdiodes becoming available. Although none were purchased to a low-leakage specification, correspondence with manufacturers indicates that some improvement in leakage could be achieved by selection.

If supply voltages above approximately 4 to 5 volts are to be used, little consideration need be given to diode forward parameters. For very low voltages, gallium arsenide diodes would offer some saving in minimum supply voltage, although other means could be used to compensate for the increased dissipation. Figure 8 shows the forward drop of the three lowest leakage diodes tested for various temperatures. The very interesting characteristic of the DGS-54 gallium arsenide diode is included as figure 7 for comparison.

COMMENTS AND CONCLUSIONS

The results of the survey indicate that there are a number of presently available transistors that are well suited to micropower circuit applications. The tests conducted on the S-4528 and S-4529 transistors indicate that high-quality planar transistors have the required stability for space applications. In evaluating the failures that did occur during testing, it should be considered that the devices were tested under rather extreme conditions and were obtained from pilot production as well as very early production runs on these devices. There is no reason to believe that these transistors, or others suitable for micropower applications, should have a higher failure rate than any other silicon planar device.

Suitability of these transistors was demonstrated by building and testing a number of logic circuits including all types of multivibrators and gates. Repetition rates as high as a megacycle were attained at low-milliwatt-power levels, less for some simple gating circuits. Flip-flops operating at several kilocycles and consuming 50 to 100 microwatts were constructed. As a test of the lower limits of power attainable, a 2-kilocycle free-running multivibrator was built that operated on less than 1 microwatt.

There is still considerable potential for improvement in micropower circuitry. Considerable gains can be made in the design of circuits more suitable for low-power operation, and secondly, there is much room for device improvement.

It must be noted that none of the transistors tested were specifically designed for micropower applications. Specifically, all are capable of dissipating hundreds of milliwatts or more. This means that their physical structure is much larger than necessary for micropower applications. Because of this condition the junction capacitances are needlessly large and the dropoff of H_{FE} at low currents is more than would be expected for a smaller geometry device. If a sufficient demand existed, it would seem that a manufacturer could produce a true micropower transistor with considerably better performance, particularly speed. This has been done on a very limited basis by CBS Laboratories for use in their own microcircuits. Data that they have released indicate much lower junction capacitances and faster operation at lower power levels in conventional circuitry. Unfortunately, the device is manufactured only as an NPN and is not for sale except in CBS's integrated circuitry.

Lewis Research Center
National Aeronautics and Space Administration
Cleveland, Ohio, October 13, 1964

APPENDIX A

TRANSISTOR CHARACTERISTIC CURVES

Figures 9 to 11 are to be used as aids to designing micropower circuitry. This appendix includes supplemental data not fully described in the body of the report. Specifically, it includes graphs of the parameters of interest for some of the transistors tested other than the S-4528 and S-4529, which were covered in detail in the main body of this report. It may be, particularly for other applications where junction capacitance is not as important, that some of these devices will be as good or better than the ones selected for our particular application.

Two devices in this category are the 2N2222 and the 2N2412. They can be used in the inverted configuration as fast, low-level switches in chopper applications.

APPENDIX B

PARAMETER MEASURING METHODS

The methods used are in most cases conventional with the following exceptions:

(1) Because of the extremely low-leakage currents being measured, all of the measuring circuit was completely shielded in a small aluminum box fitted with a coaxial connector for connection to the electrometer shown (see fig. 12). Further shielding was provided by placing a metal shield over the transistor under test. During the tests precautions were taken not to handle the transistor with the hands in order to keep the transistor case temperature constant. The 1-kilohm resistor across the power supplies provided a small load to the power supply to increase its output stability.

(2) The collector-base and emitter-base capacitances were measured using the setup shown schematically in figure 13. The 20-kilohm resistance shunting the capacitance meter is used to reduce the alternating-current voltage impressed across the junction from approximately 1.1 to 0.3 volts peak to peak. This reduction in voltage prevents the alternating-current waveform from being clipped by the transistor junction diode and thus provides a more accurate reading of capacitance. The measuring frequency is in the range of 120 to 140 kilocycles.

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TABLE I. - MEASURED PARAMETER AVERAGES FOR SOME NPN SILICON TRANSISTORS

Transistor type	Manufacturer	Lot size	Process	Collector-base leakage current at collector-base voltage of 10 v, I_{CBO}, na	Emitter-base leakage current at base-emitter voltage of 3 v, I_{EBO}, na	Collector current, I_C, μamp: Direct-current gain, H_{FE} (a) 10	100	1000	Base-emitter voltage at base current of 1 μamp, V_{BE}, v	Input capacitance at base-emitter voltage of 0 v, C_{ie}, pf	Output capacitance at collector-base voltage of 0 v, C_{ob}, pf	Base current, I_B, μamp: Average ΔV (-25° to +75° C), mv/°C (b) 5	50
S-4529	Fairchild	100	Planar	0.04	1.0	60	105	145	0.513	6.4	7.1	1.71	1.54
2N1613	↓	6	↓	.05	.007	29	39	49	.536	71	53	----	----
2N917		4		.02	.005	11	20	33	.606	2.2	2.4	----	----
2N338	General Electric	10	Grown junction diffused base	0.24	1,400	16	39	84	0.530	14.3	5.1	----	----
2N1276	↓	2	↓	3.0	55,000	2.2	6.0	12	.414	29.6	7.6	----	----
2N1277		10		1.0	10,000	4.5	13	25	.479	18.4	5.1	----	----
2N1278		10		.18	11,000	13	27	41	.513	23.2	5.4	----	----
2N1279		6		.25	350	2.3	55	121	.539	12.8	5.6	----	----
MM445	Motorola	10	Double diffused epitaxial	7.8	16	6.1	12	31	0.495	5.5	3.9	----	----
MM513	↓	4	Star planar	.007	1.3	69	92	--	.555	21.5	11.5	----	----
2N2222		100	↓	.04	2.5	32	50	--	.540	24.3	14.6	1.85	1.69
NS435	National	5	Diffused mesa	0.34	0.08	50	110	170	0.538	7.5	7.9	----	----
2N760A	↓	6	↓	.36	.29	14	31	67	.502	9.8	9.3	----	----
2N706	Radio Corporation of America	6	Double diffused mesa	6.2	92	5.3	11	21	0.532	9.1	10.7	1.80	1.61
TI490	Texas Instruments	6	Double diffused mesa	0.05	0.07	27	41	70	0.539	9.4	4.9	----	----
[c]2N929	↓	20	Planar	.02	.04	71	95	120	.570	10.3	10.9	1.83	1.62
[c]2N930		10	↓	.03	.25	149	201	273	.557	11	11.5	1.85	1.63
2N2432		5		.016	.023	100	166	234	.560	4.0	6.4	1.80	1.53
ME?00A	Advanced Microelectronics	4	Planar	0.014	0.0015	80	180	283	0.553	7.7	6.7	----	----

[a] Value of H_{FE} are interpolated from data taken at constant base current.

[b] Average of three samples.

[c] 2N929 and 2N930 are similar transistors that differ only in H_{FE}.

TABLE II. - MEASURED PARAMETER AVERAGES FOR SOME PNP SILICON TRANSISTORS

Transistor type	Manufacturer	Lot size	Process	Collector-base leakage current at collector-base voltage of -10 v, I_{CBO}, na	Emitter-base leakage current at base-emitter voltage of -3 v, I_{EBO}, na	Collector current, I_C, μamp: 10	100	1000	Base-emitter voltage at base current of 1 μamp, V_{BE}, v	Input capacitance at base-emitter voltage of 0 v, C_{ie}, pf	Output capacitance at collector-base voltage of 0 v, C_{ob}, pf	Base current, I_B, μamp: 5	50
						Direct-current gain, H_{FE} (a)						Average ΔV (-25° to +75° C), mv/°C (b)	
2N1640	Crystalonics	8	Alloy junction	0.40	0.11	4.1	5.0	7.2	0.398	53	51	----	----
S4528	Fairchild	20	Planar	0.030	2.6	50	82	114	0.584	7.7	12.8	----	----
HA9038	Hughes	18	Double diffused mesa	1.3	0.13	33	60	87	0.565	15.6	18.1	2.00	1.72
2N1257	↓	8	↓	7.3	.98	16	27	43	.536	21.6	21.6	----	----
2N1259		6		2.1	15	12	22	38	.513	21.9	20.4	----	----
2N1443	National	4	Alloy junction	1.6	0.19	16	35	61	0.457	8.4	16.5	----	----
T2071	Philco	20	Precision alloy	2.2	1.0	16	34	--	0.542	20.7	11.2	----	----
2N865	↓	6	Precision alloy	3.2	9.2	8.1	22	54	.422	8.1	11.7	----	----
2N1429		4	Surface alloy	12	4.8	6.3	20	31	.458	8.3	16	----	----
2N1676	↓	5	Surface alloy	13	30	6.4	19	41	.488	11.1	17.5	----	----
[c]262S2	Sperry	28	Alloy junction	1.1	0.13	36	77	--	0.484	8.6	17.7	----	----
[c]285S2	↓	10	↓	.10	.04	41	87	133	.502	7.0	16.3	----	----
2N2412	Texas Instruments	6	Epitaxial planar	1.5	0.00025	33	42	53	0.603	4.8	7.9	1.80	1.61

[a]Value of H_{FE} are interpolated from data taken at constant base current.

[b]Sample of one.

[c]Selected to tighter spaces; from the family of transistors that includes the 2N941.

TABLE III. - PUBLISHED SPECIFICATIONS OF TRANSISTOR S-4528 (PNP)

(a) Maximum rating at 25° C

Characteristic	
Collector-base voltage, V_{CBO}, v	-15
Collector-emitter voltage, V_{CEO}, v	-10
Emitter-base voltage, V_{EBO}, v	-2
Total dissipation	
At case temperature of 25° C, w	1.2
At case temperature of 100° C, w	.68
At ambient temperature of 25° C, w	.36

(b) Electrical properties at 25° C

Characteristic	Maximum	Minimum	Test conditions
Direct-current pulse gain, H_{FE}	--------	25	I_C = 0.010 ma, V_{CE} = -1.0 v
Collector saturation voltage, V_{CE}(sat)	-1.0 v	-----	I_C = 1.0 ma, I_B = 0.1 ma
Base saturation voltage, V_{BE}(sat)	-1.0 v	-----	I_C = 0.1 ma, I_B = 0.1 ma
Collector-base cutoff current, I_{CBO}	10 namp	-----	V_{CB} = 10 v, I_E = 0
	1.0 μamp	-----	V_{CB} = -10 v, T = 100° C
High-frequency current gain, H_{fe} (f = 50 mc)	--------	1.0	V_{CE} = -7.0 v, I_C = 10 ma
Output capacitance, C_{ob}	9 pf	-----	I_E = 0, V_{CB} = -10 v
Emitter transition capacitance, C_{te}	11 pf	-----	I_C = 0, V_{EB} = -0.5 v

TABLE IV. - PUBLISHED SPECIFICATIONS OF TRANSISTOR S-4529 (NPN)

(a) Maximum rating at 25° C

Characteristic	
Collector-base voltage, V_{CBO}, v	15
Collector-emitter voltage, V_{CEO}, v	10
Emitter-base voltage, V_{EBO}, v	2
Total dissipation	
At case temperature of 25° C, w	1.2
At case temperature of 100° C, w	.68
At ambient temperature of 25° C, w	.36

(b) Electrical properties at 25° C

Characteristic	Maximum	Minimum	Test conditions
Direct-current pulse gain, H_{FE}	-----	40	I_C = 0.010 ma, V_{CE} = 1.0 v
Collector-emitter saturation voltage, V_{CE}(sat)	1.0 v	--	I_C = 1.0 ma, I_B = 0.1 ma
Base-emitter saturation voltage, V_{BE}(sat)	1.0 v	--	I_C = 1.0 ma, I_B = 0.1 ma
Collector-base cutoff current, I_{CBO}	10 namp	--	V_{CB} = 60 v, I_E = 0
	1.0 μamp	--	V_{CB} = 10 v, I_E = 0, T = 100° C
High-frequency current gain, H_{fe}	----	1.0	I_C = 10 ma, V_{CE} = 7.0 v
Output capacitance, C_{ob}	3.5 pf	---	I_E = 0, V_{CB} = 10 v
Emitter transition capacitance, C_{te}	9 pf	---	I_C = 0, V_{BE} = 0.5 v

TABLE V. - STRESSING TEST DATA FOR TRANSISTOR TYPES S-4528 AND S-4529

Transistor type	Lot	Size	Date received	Stressing profile (storage times are nominal)	Catastrophic failures (a)	Degradation failure: Collector-base leakage current, I_{CBO} (b)	Degradation failure: Emitter-base leakage current, I_{EBO} (b)	Degradation failure: Direct-current gain, H_{FE} (c)	Time interval in which failures were noted
S4529 (NPN)	A	20	January 17, 1962	63 Temperature cycles[d]	0	0	0	0	----------
	B	20		63 Temperature cycles plus 1000-hour storage at 200° C	0	1	1	0	I_{CBO}, 20 - 40 cycles I_{EBO}, 498 - 1002 hr
	C	20		1000-Hour storage at 200° C	0	0	0	0	----------
	D	20		100-Hour storage at 200° C plus 1-week storage at room temperature plus 1000-hour storage at 200° C	0	0	0	0	----------
	E	20		1000-Hour storage at room temperature, control lot	0	0	0	0	----------
S4528 (PNP)	F	20	March 23, 1962	1000-Hour storage at 200° C	0	1	0	0	I_{CBO}, 168 - 336 hr
	H	70	July 10, 1962	1108-Hour storage at 200° C[e]	[f]1	4	0	3	H_{FE}: 0-168, 168-648, 1008-1104 I_{CBO}: 0-648, 168-648, 168-648, 840-1008 Open: 648-840

[a] Catastrophic failure defined as inoperable unit, i.e., open or short between terminals.

[b] Leakage degradation defined as increase of 200 percent or greater from initial value.

[c] Degradation of H_{FE} defined as decrease of 25 percent or greater from initial value.

[d] Temperature cycle, 15 min at -55° C, 30 min at 200° C; total cycle time including transients, 1 hr.

[e] Precycled five times.

[f] Emitter base open.

TABLE VI. - STABILITY OF COLLECTOR-BASE LEAKAGE CURRENT

[Temperature, 25° C; $|V_{CB}|$ = 10 v.]

Lot	Initial leakage, amp			Final leakage, amp		
	Percentile					
	10th	50th	90th	10th	50th	90th
A	22×10^{-12}	32×10^{-12}	69×10^{-12}	25×10^{-12}	37×10^{-12}	79×10^{-12}
B	21	28	48	27	38	80
C	25	30	120	23	31	130
D	23	31	74	25	35	79
E	19	32	57	22	36	59
F	9.5	19	61	5.0	13	67
H	3.3	6.9	630	2.1	3.6	670

TABLE VII. - STABILITY OF DIRECT-CURRENT GAIN H_{FE}

[Temperature, 25° C; base current, 0.5 μamp; $|V_{CE}|$ = 4.5 v.]

Lot	Initial			Final		
	Percentile					
	10th	50th	90th	10th	50th	90th
A	64	83	130	63	81	130
B	63	85	110	71	94	115
C	65	81	125	68	93	133
D	64	86	133	69	88	138
E	60	78	144	62	78	145
F	19	55	112	25	65	142
H	34	83	165	39	86	177

TABLE VIII. - STABILITY OF EMITTER-BASE LEAKAGE CURRENT

[Temperature, 25° C; $|V_{EB}|$ = 3 v.]

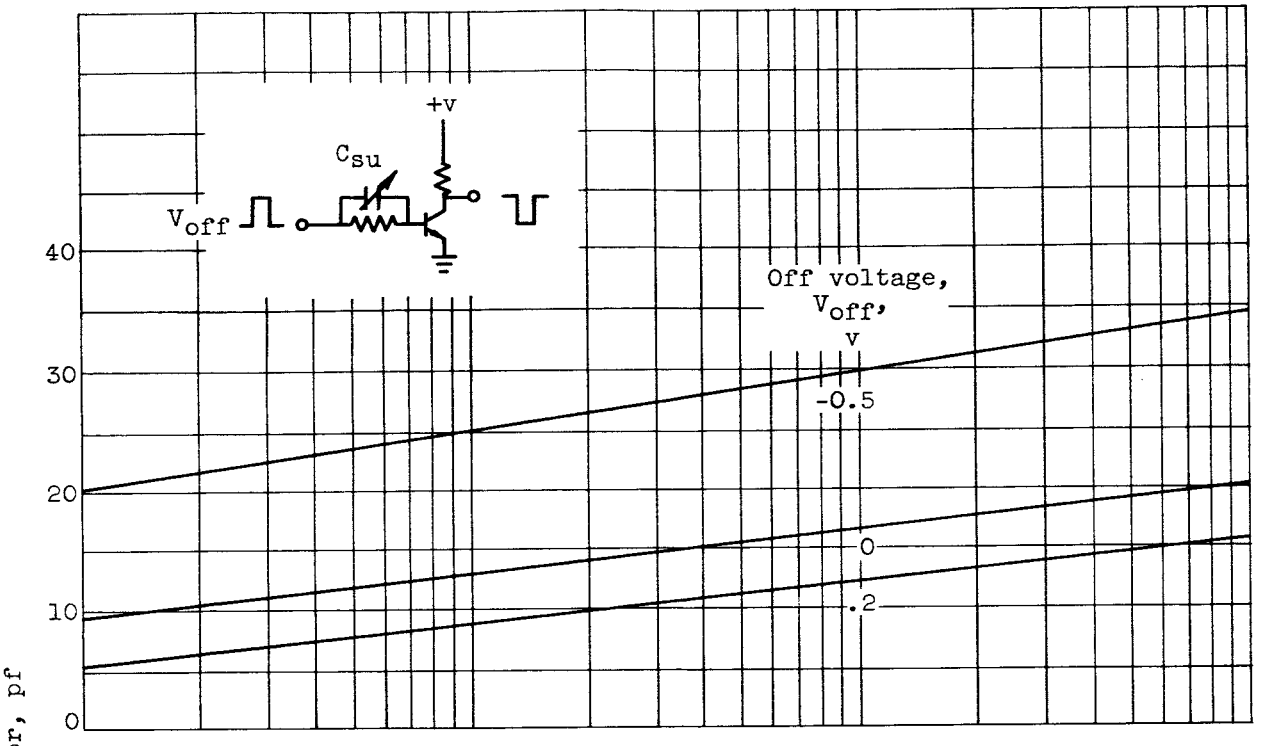
Lot	Initial current, amp			Final current, amp		
	Percentile					
	10th	50th	90th	10th	50th	90th
A	0.25×10^{-9}	0.53×10^{-9}	1.6×10^{-9}	0.22×10^{-9}	0.54×10^{-9}	1.5×10^{-9}
B	.15	.55	5.0	.19	.59	5.1
C	.39	.73	2.9	.35	.65	2.3
D	.32	.78	6.7	.37	.85	4.9
E	.20	.71	1.7	.19	.65	1.7
F	.60	2.1	3.5	.60	2.1	3.5
H	3.2	7.6	28	2.8	7.3	27

TABLE IX. - MEASURED CHARACTERISTICS OF SOME SILICON DIODES

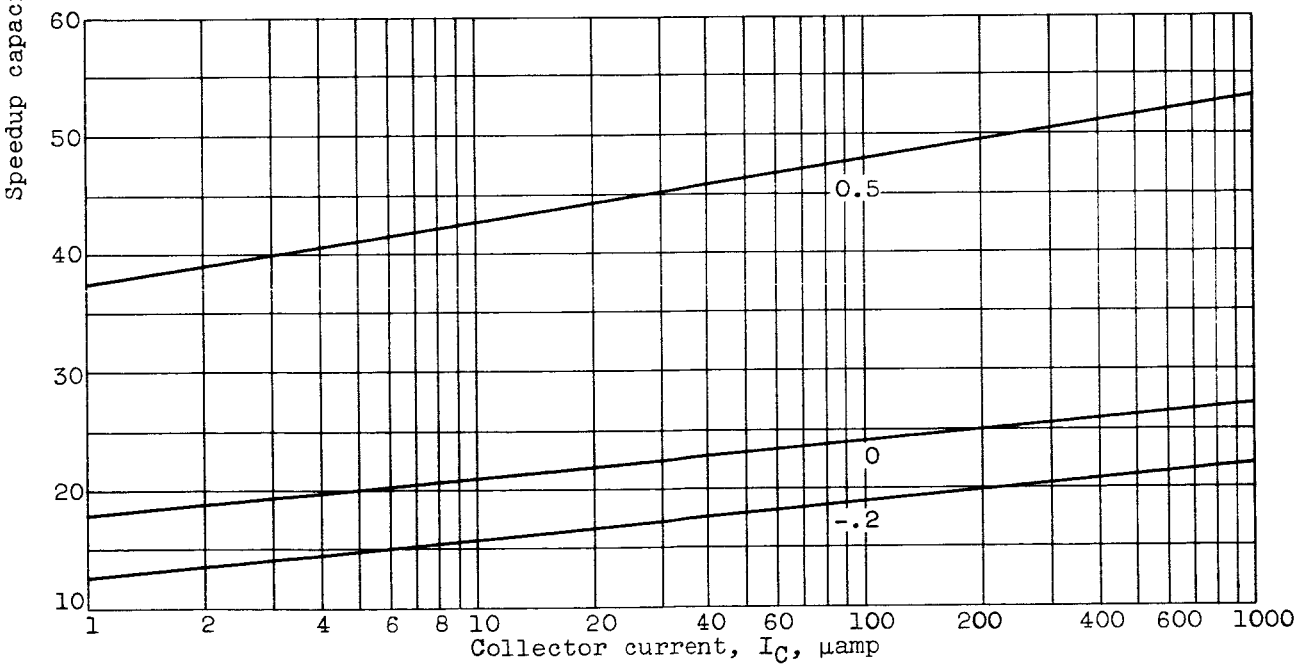
Diode type	Manufacturer	Lot size (a)	Leakage current at 10 v average	Average capacitance at 0 v, C_O, pf	Temperature, 25° C				Forward current, I_F, μamp	
					Forward current, I_F, μamp				5	50
					5	50	5	50	Temperature coefficient, mv/°C	
					Forward voltage, V_F, v		Change in forward voltage, ΔV_F, v			
FD300	Fairchild	5	0.13×10^{-9}	4.4	0.423	0.505	0.061	0.087	2.54	2.31
FD600		7	12	1.34	.327	.442	.027	.083	2.86	2.47
1N3728	Raytheon	7	0.19×10^{-9}	4.9	0.421	0.508	0.006	0.010	2.56	2.24
1N483		4	4.7	4.42	.392	.479	.027	.022	2.60	2.37
1N457	Hughes	8	0.54×10^{-9}	10.6	0.441	0.517	0.025	0.025	2.57	2.33
1N628		10	5.0	5.3	.407	.490	.040	.066	2.71	2.44
[b]1N3608	General Electric	7	2.7×10^{-9}	1.62	0.392	0.493	0.035	0.024	2.46	2.15
TI616	Texas Instruments	5	2.9×10^{-9}	16.7	0.507	0.583	0.017	0.015	2.42	2.14
[b]IN3593		8	3.3	2.08	.412	.486	.062	.113	2.42	2.21
1N483	Transitron	4	3.4×10^{-9}	11.3	0.432	0.508	0.023	0.032	2.52	2.31
[b]1N897	Pacific Semiconductor	5	14×10^{-9}	6.73	0.369	0.468	0.021	0.015	2.71	2.41
[b]PD307		5	15	3.7	.366	.465	.077	.063	2.43	2.20

[a]Temperature coefficient, forward voltage, and change in forward voltage were determined on on random sample of three diodes.

[b]Microminiature package.



(a) Fairchild S-4529 (NPN) transistor 64; saturated operation, I_C/I_B, 50.



(b) Fairchild S-4528 (PNP) transistor 125; saturated operation, I_C/I_B, 25.

Figure 1. - Required speedup capacitor as function of collector current. Input pulse, 2.0 volts; collector supply voltage, 1.0 volt.

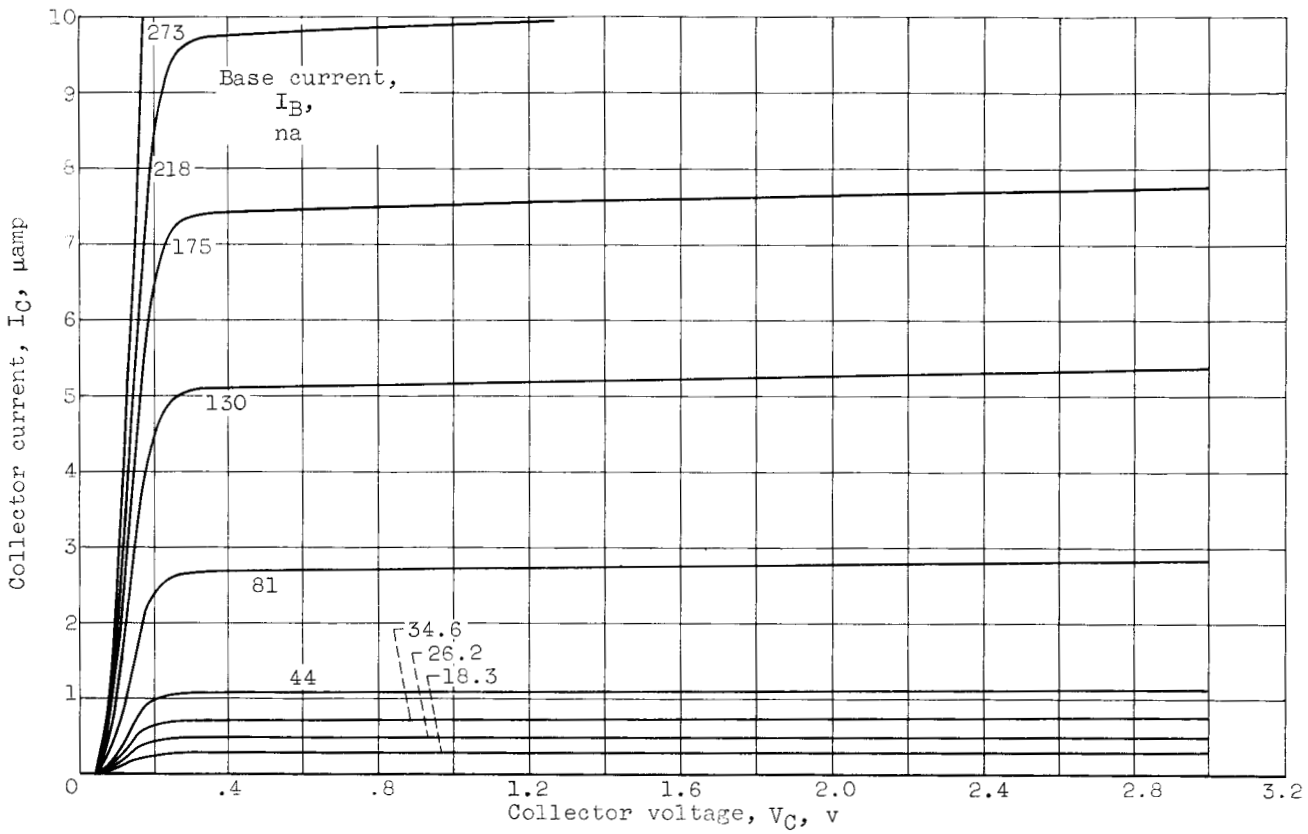
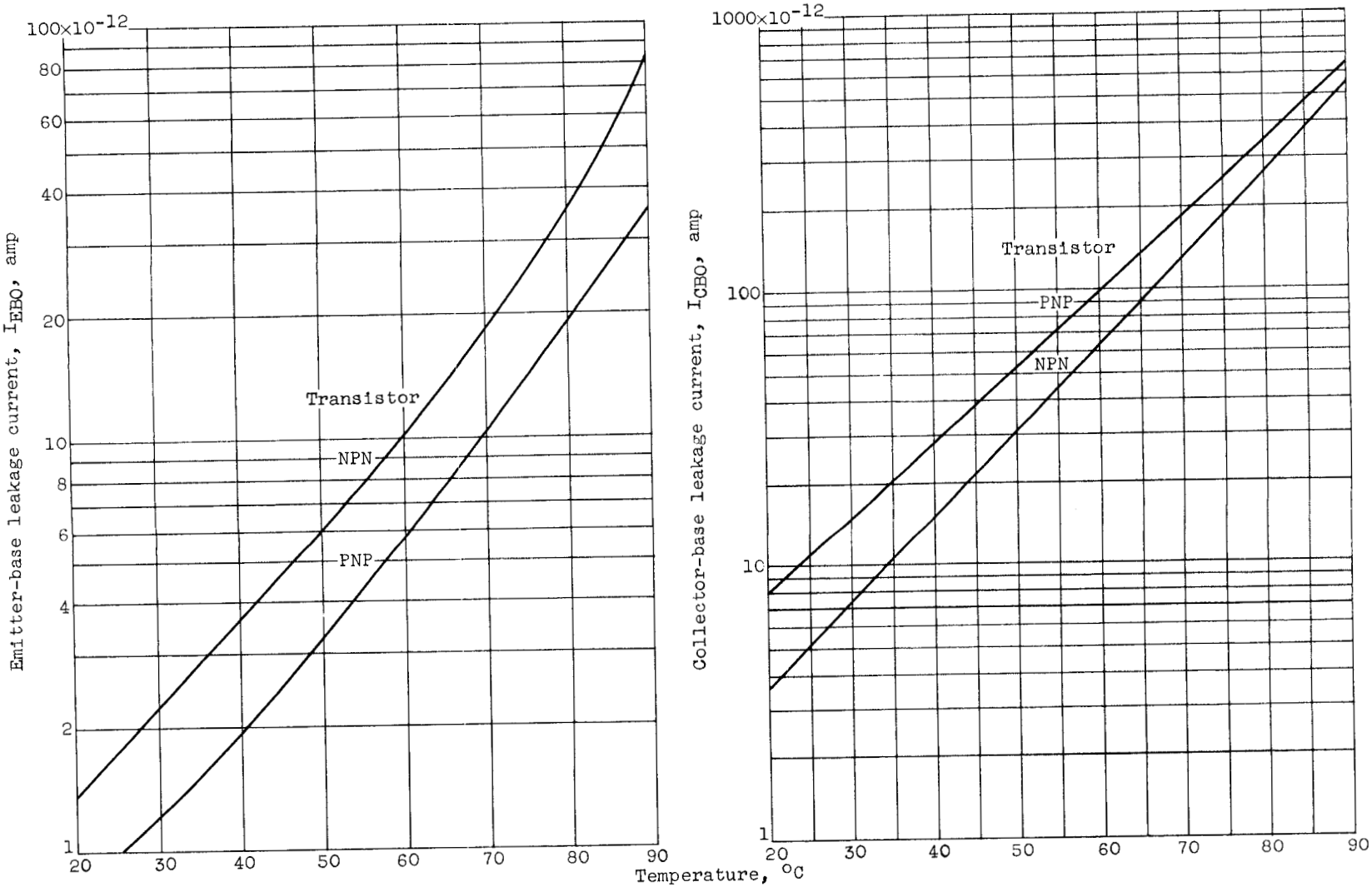


Figure 2. - Low-current collector characteristics (common-emitter). Fairchild S-4529 (NPN) transistor.



(a) Base-emitter voltage, 1 volt.

(b) Collector-base voltage, 3.0 volts.

Figure 3. - Typical transistor leakage as function of temperature. Fairchild planar passivated transistors, S-4529 (NPN) and S-4528 (PNP).

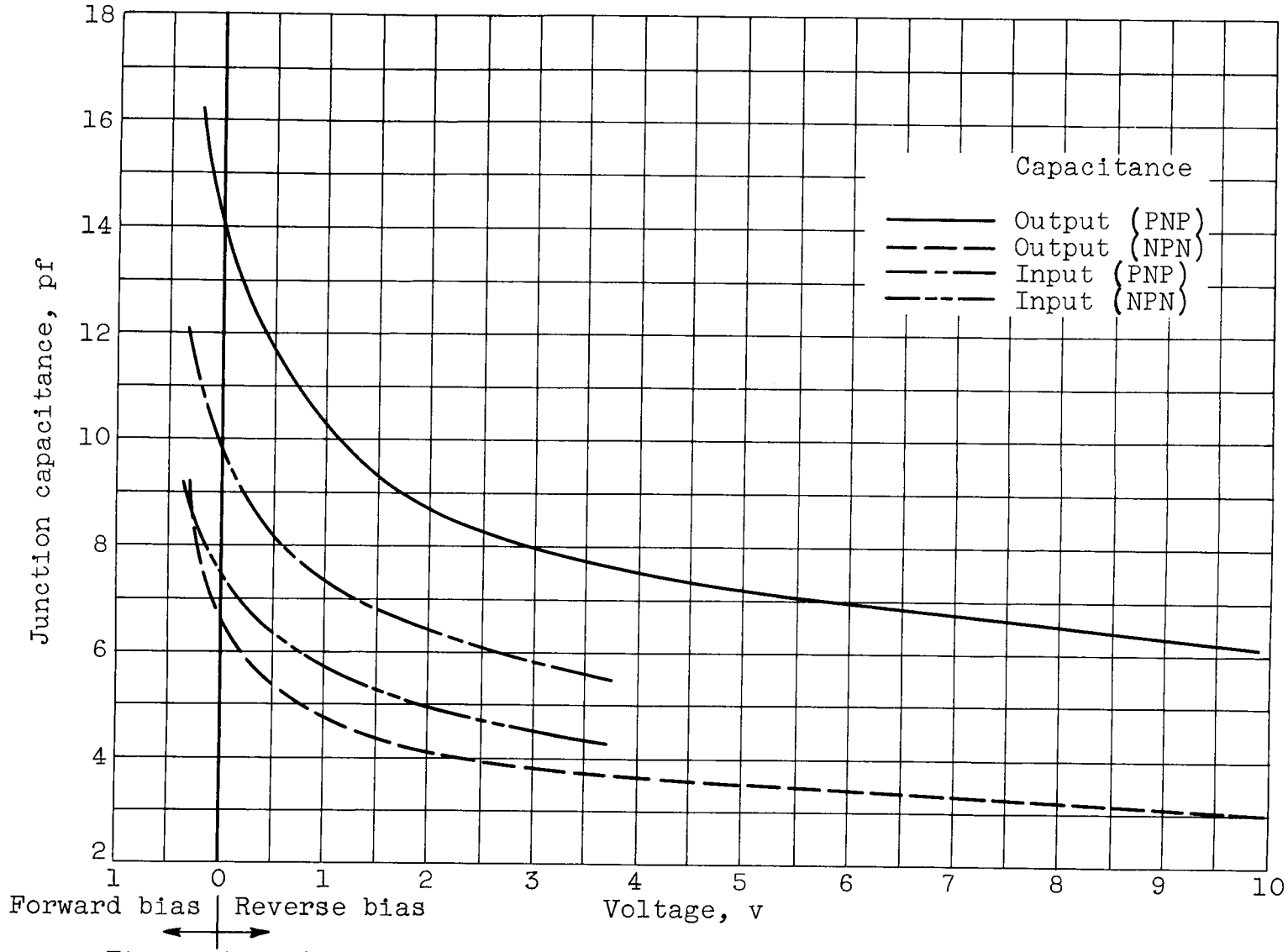
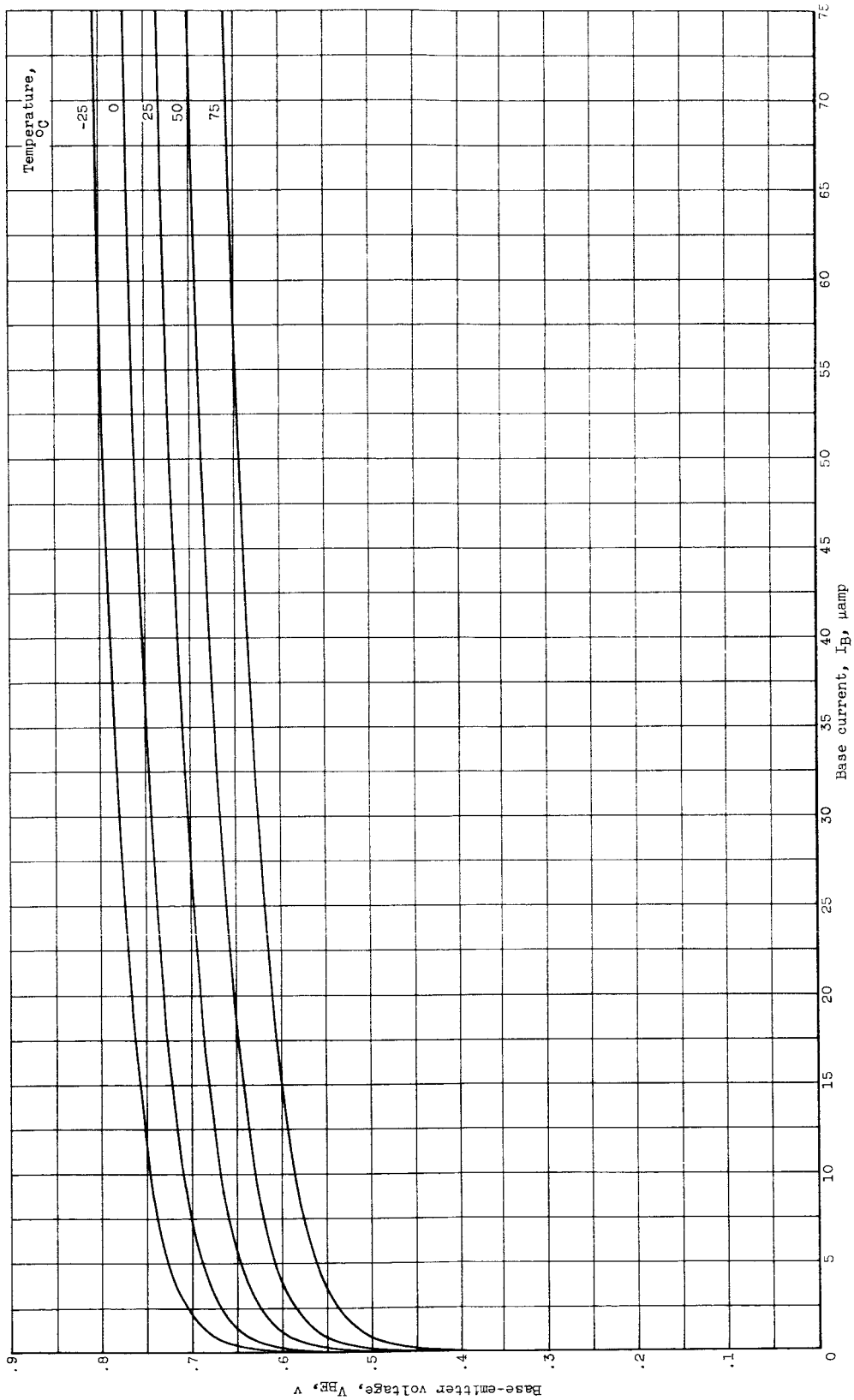
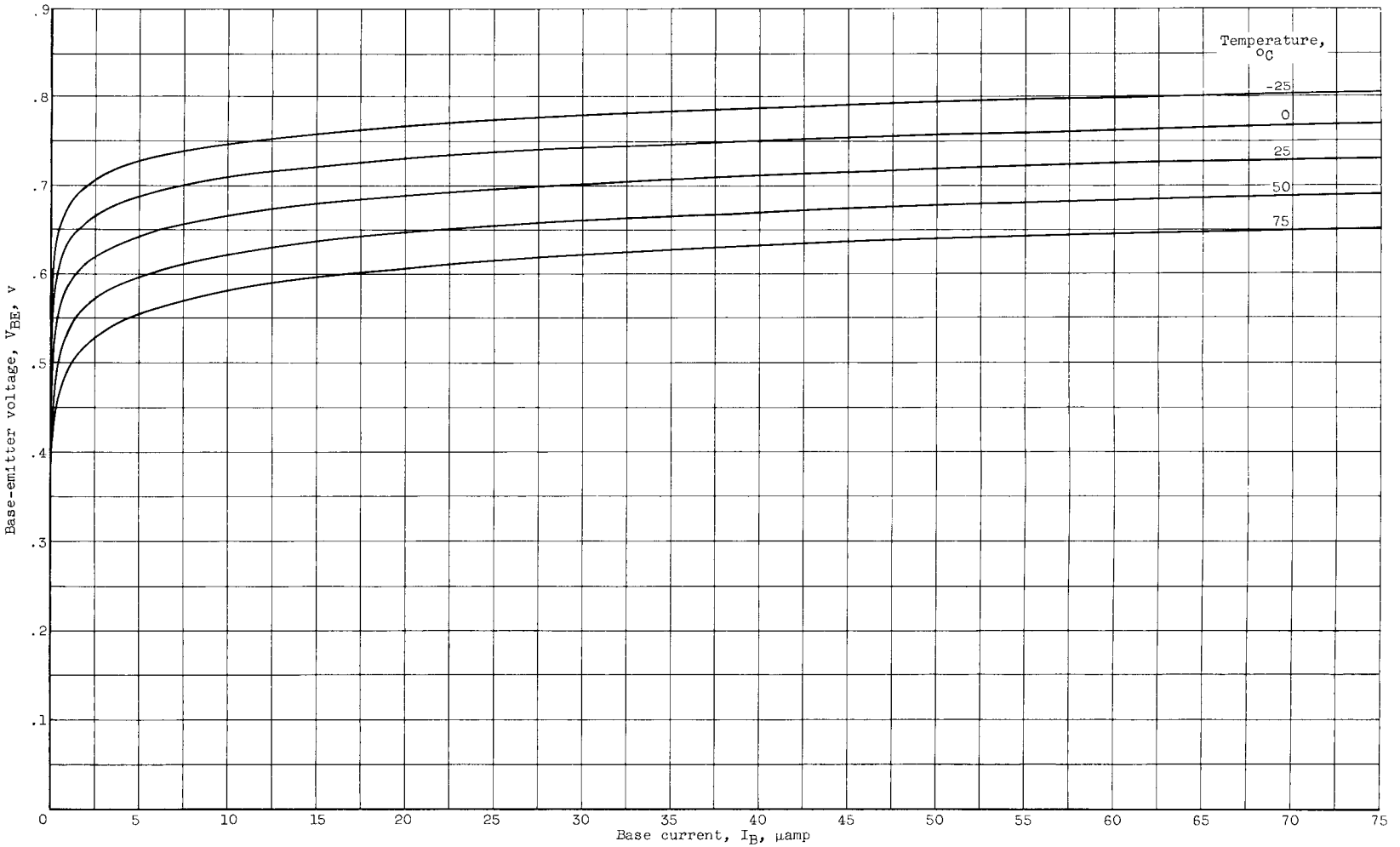


Figure 4. - Output and input capacitances as functions of bias voltage. Fairchild S-4528 (PNP) and S-4529 (NPN) transistors.



(a) Type 3-4528 (PNP).

Figure 5. - Typical base-emitter voltage characteristics of silicon transistor.



(b) Type S-4529 (NPN).

Figure 5. - Concluded. Typical base-emitter voltage characteristics of silicon transistor.

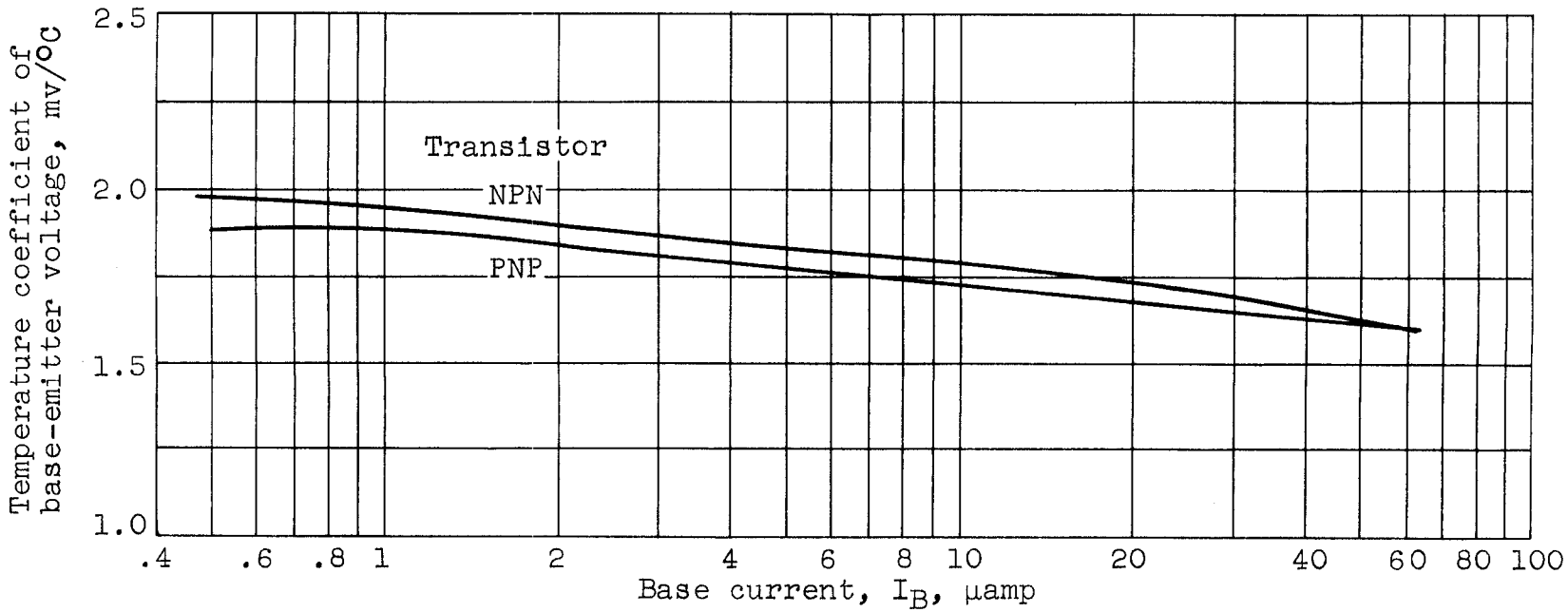


Figure 6. - Average temperature coefficient of base-emitter voltage for Fairchild S-4528 (PNP) and S-4529 (NPN) transistors. Temperature range, -20° to 80° C.

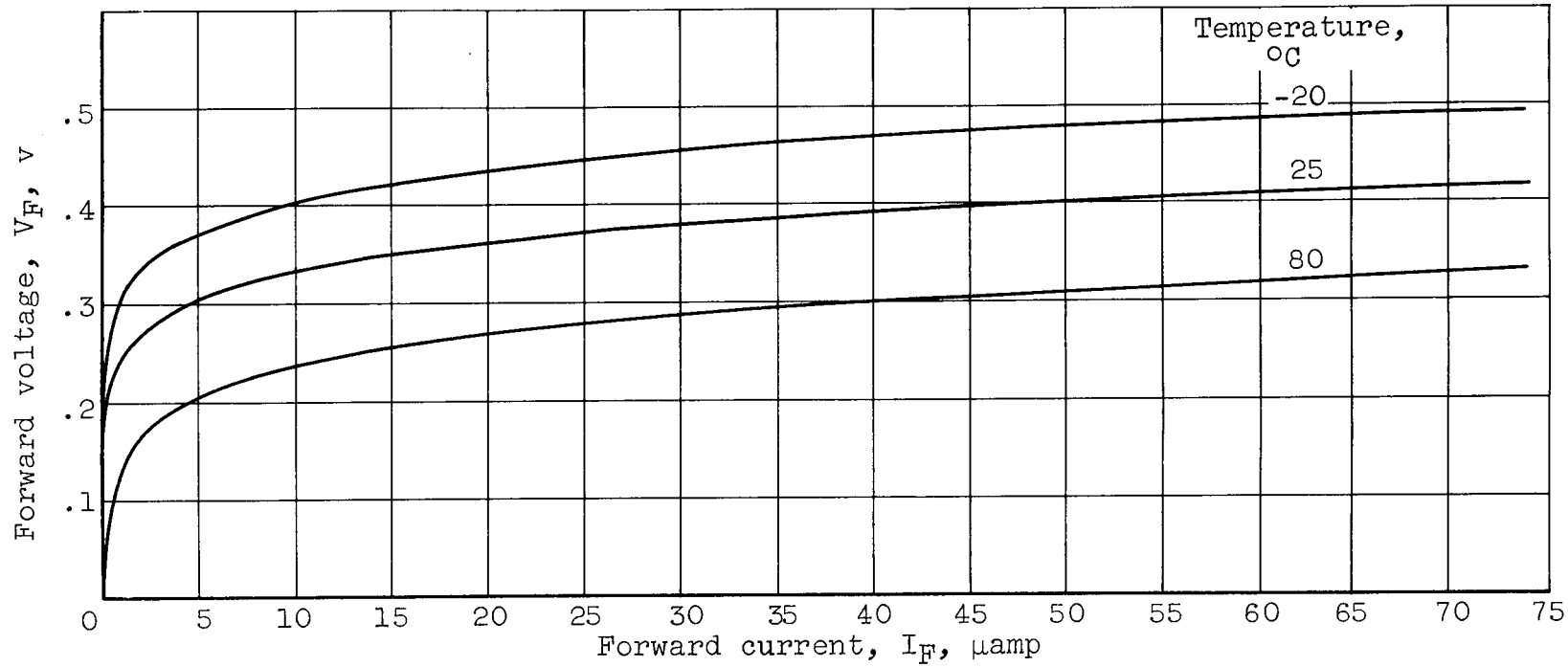
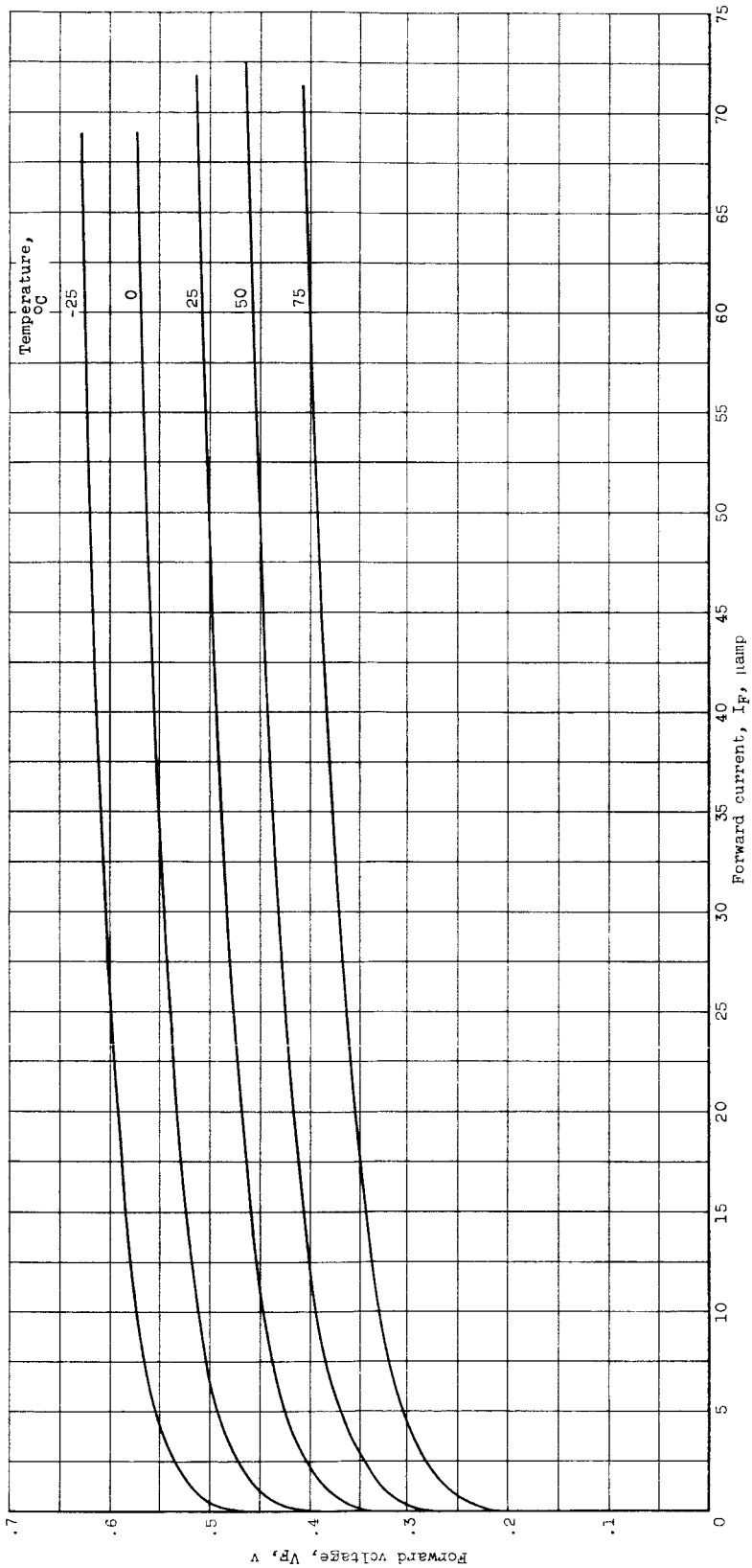
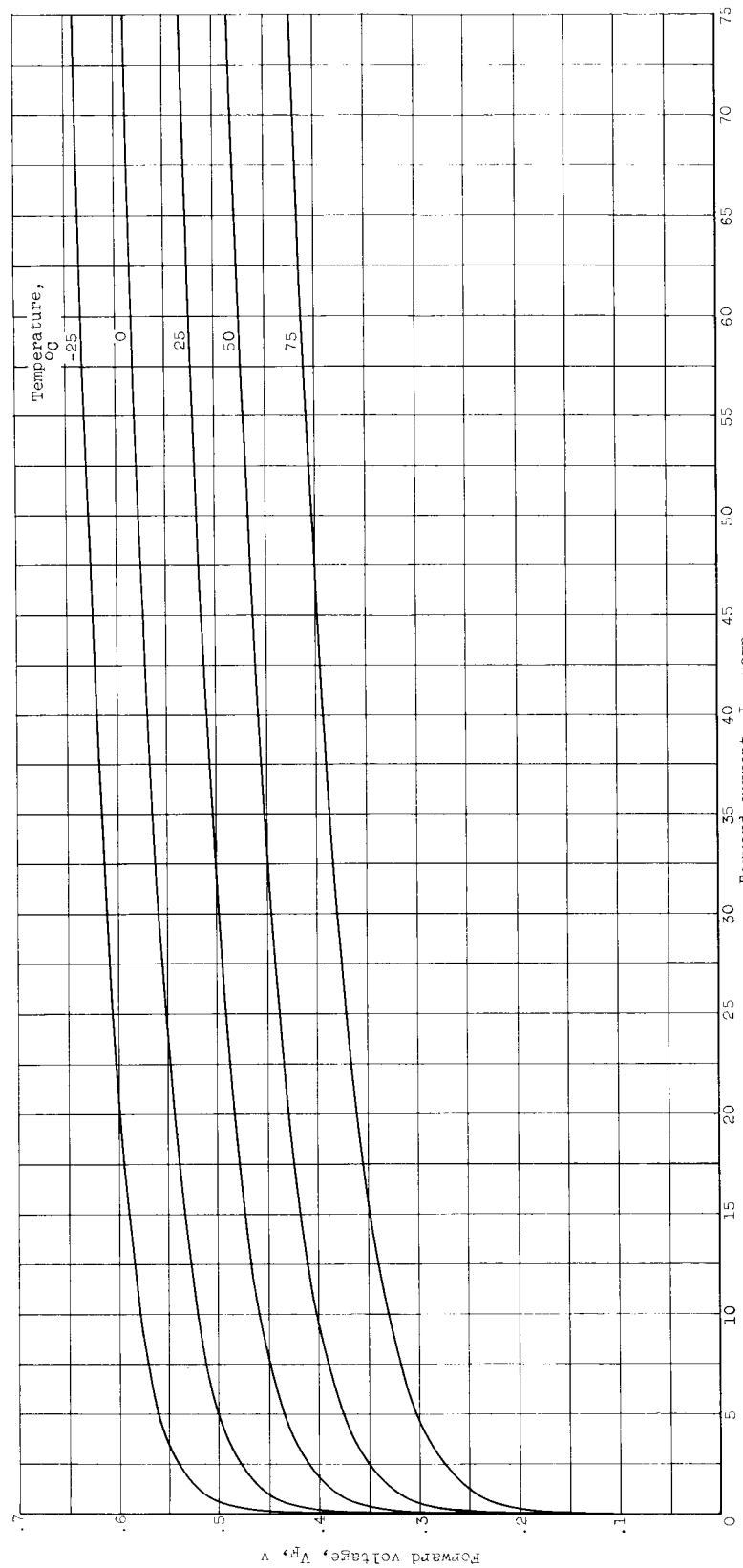


Figure 7. - Forward characteristics of gallium arsenide diode DGS-54 (Diotron).



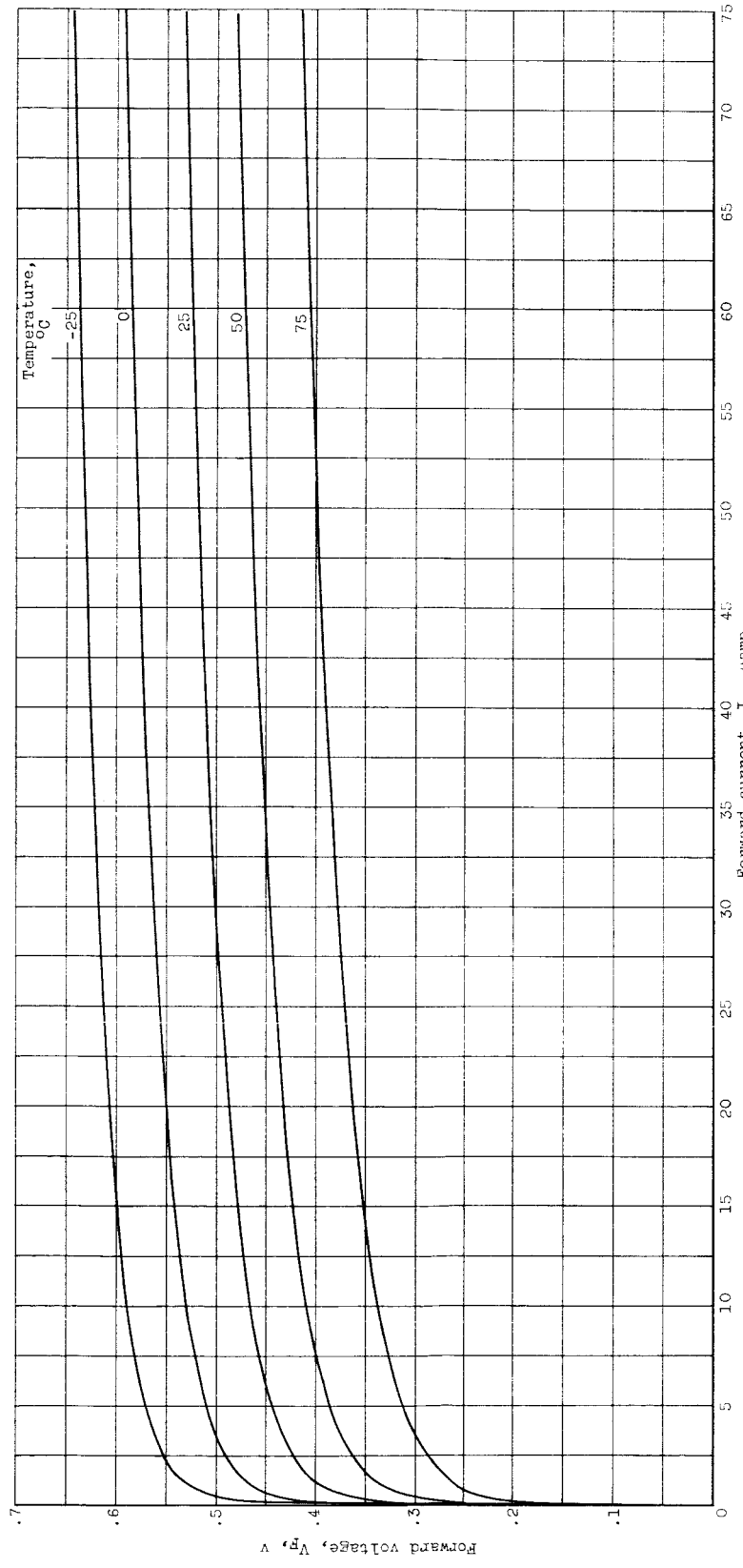
(a) Type FD-300.

Figure 8. - Forward characteristic of silicon diode.



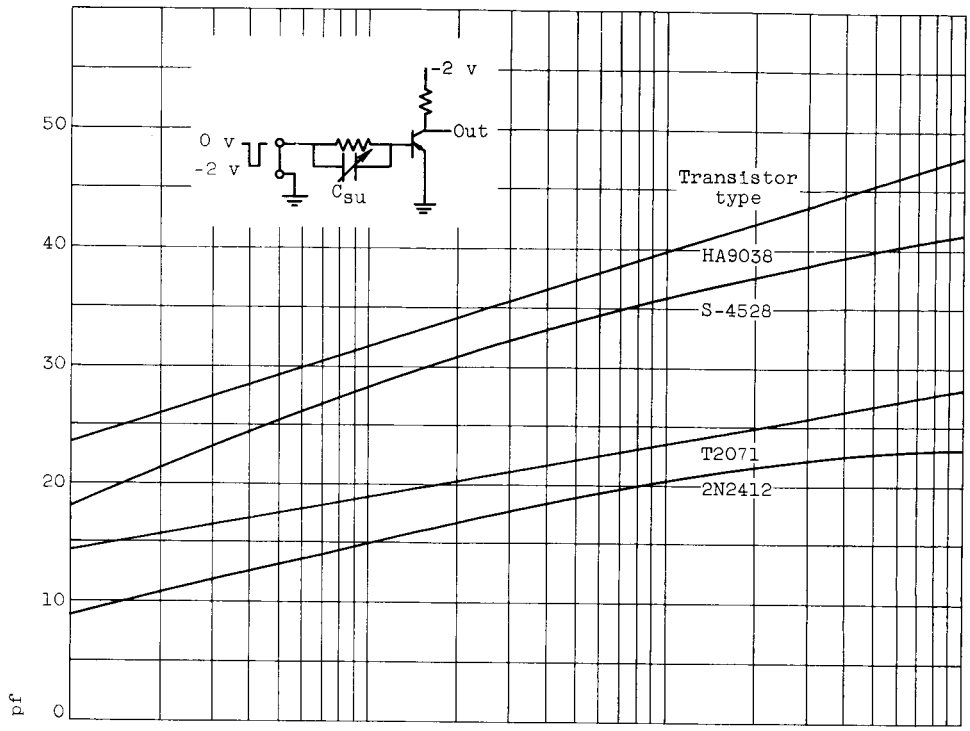
(b) Type 1N3728.

Figure 8. - Continued. Forward characteristic of silicon diode.

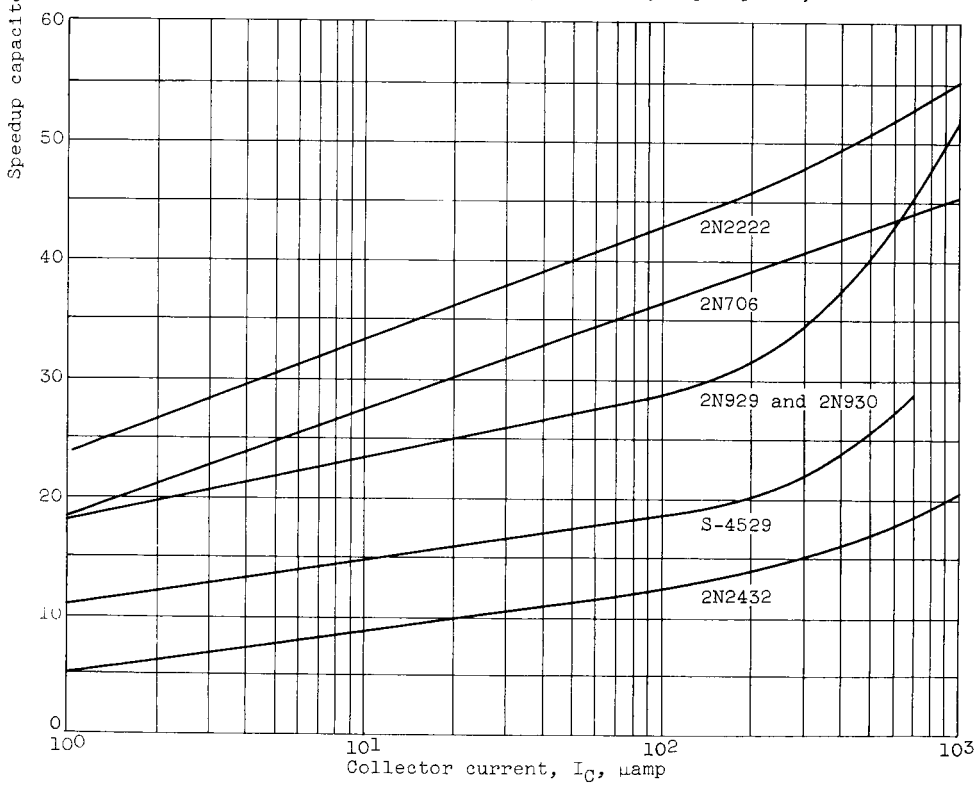


(e) Type 1N457.

Figure 8. - Concluded. Forward characteristic of silicon diode.

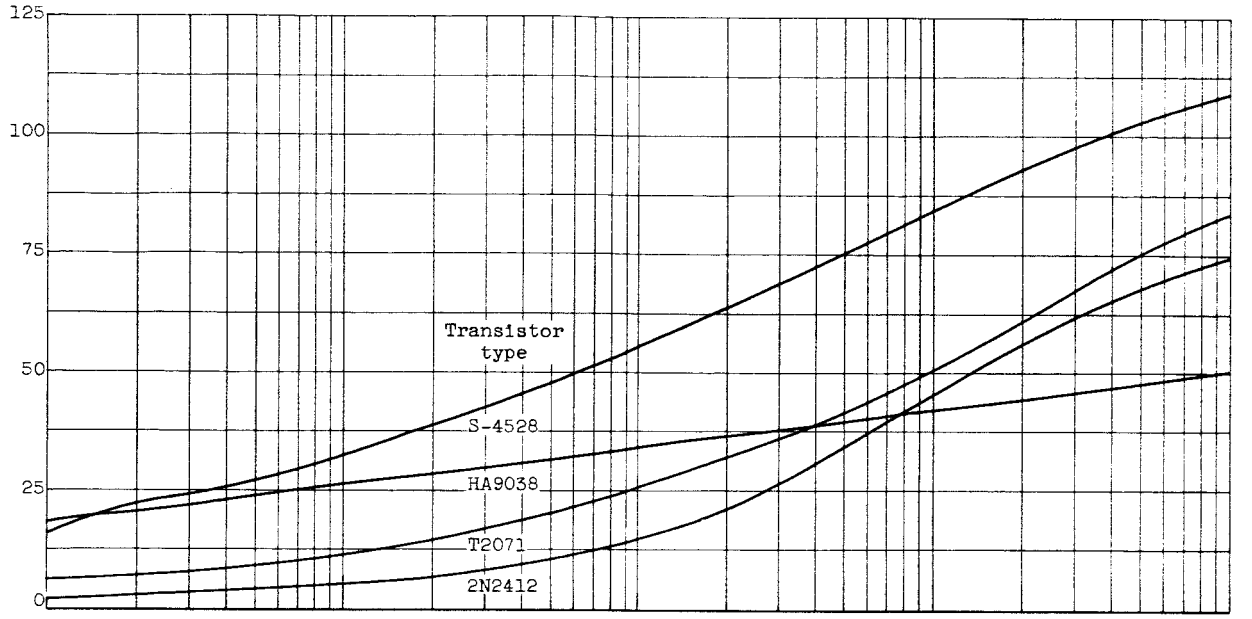


(a) PNP transistor. Collector supply, -2 volts; input pulse, -2 volts.

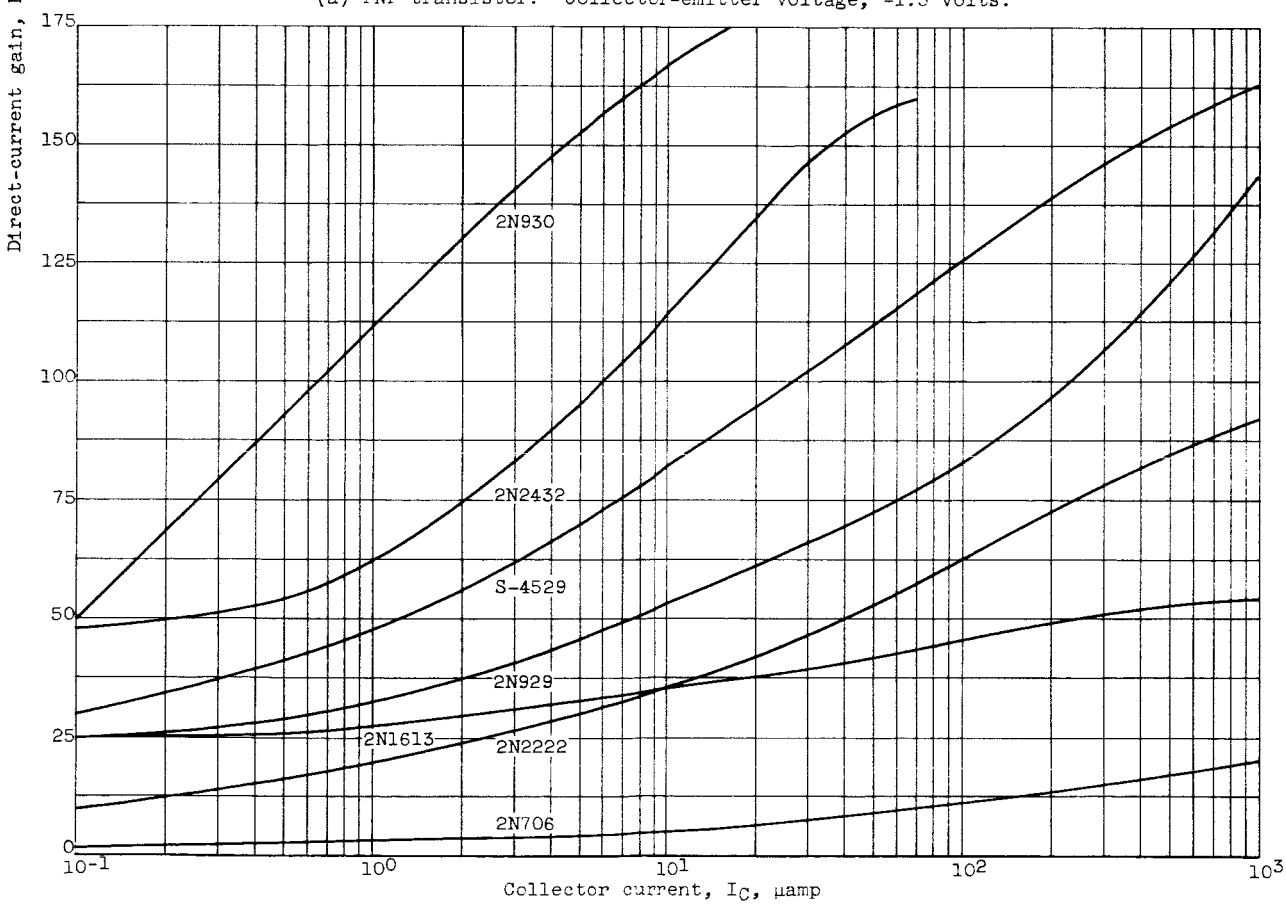


(b) NPN transistor. Collector supply, 3 volts; input pulse, 2 volts.

Figure 9. - Speedup capacitor for various collector currents. Forced direct-current gain approximately half actual direct-current gain; off voltage, 0.

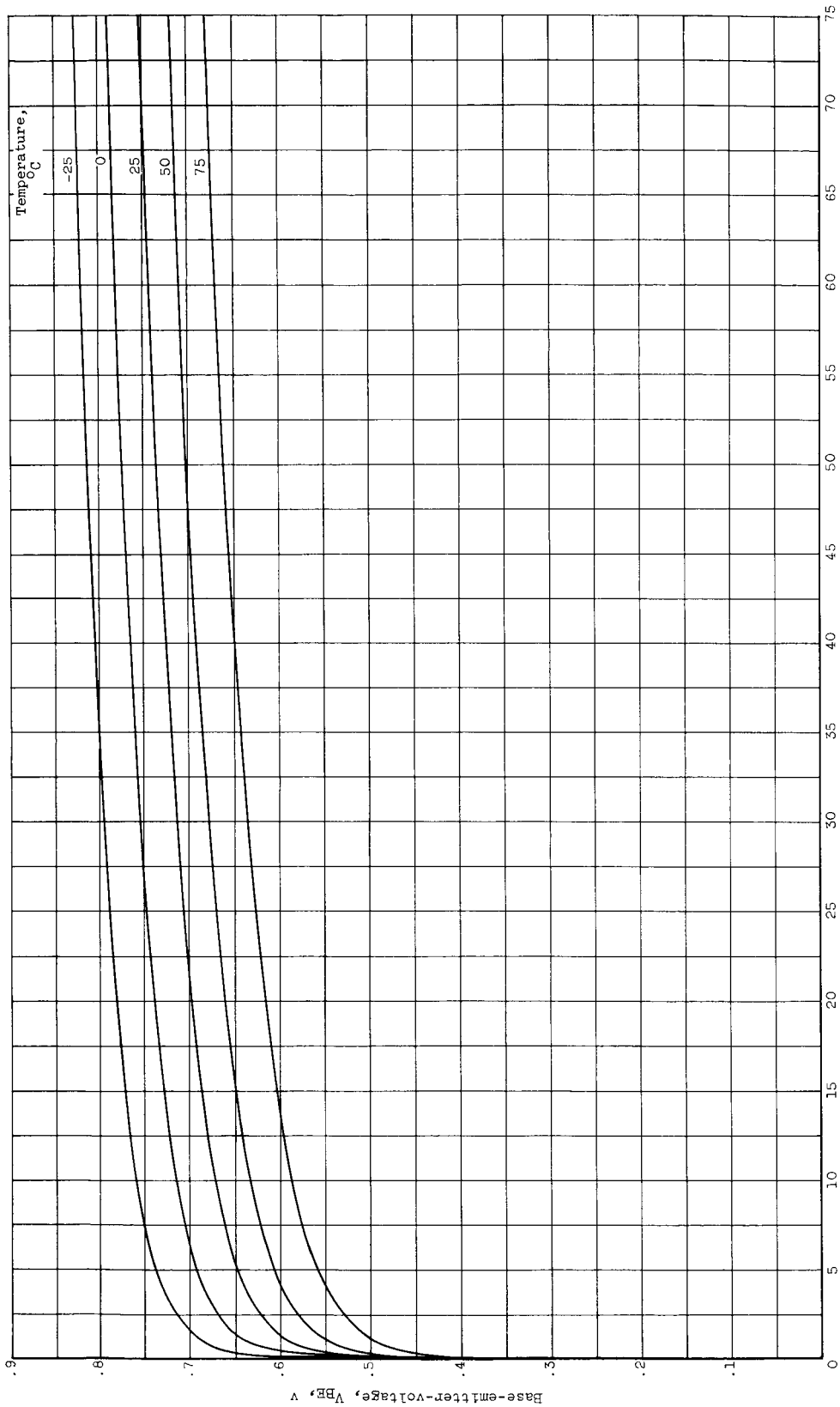


(a) PNP transistor. Collector-emitter voltage, -1.5 volts.



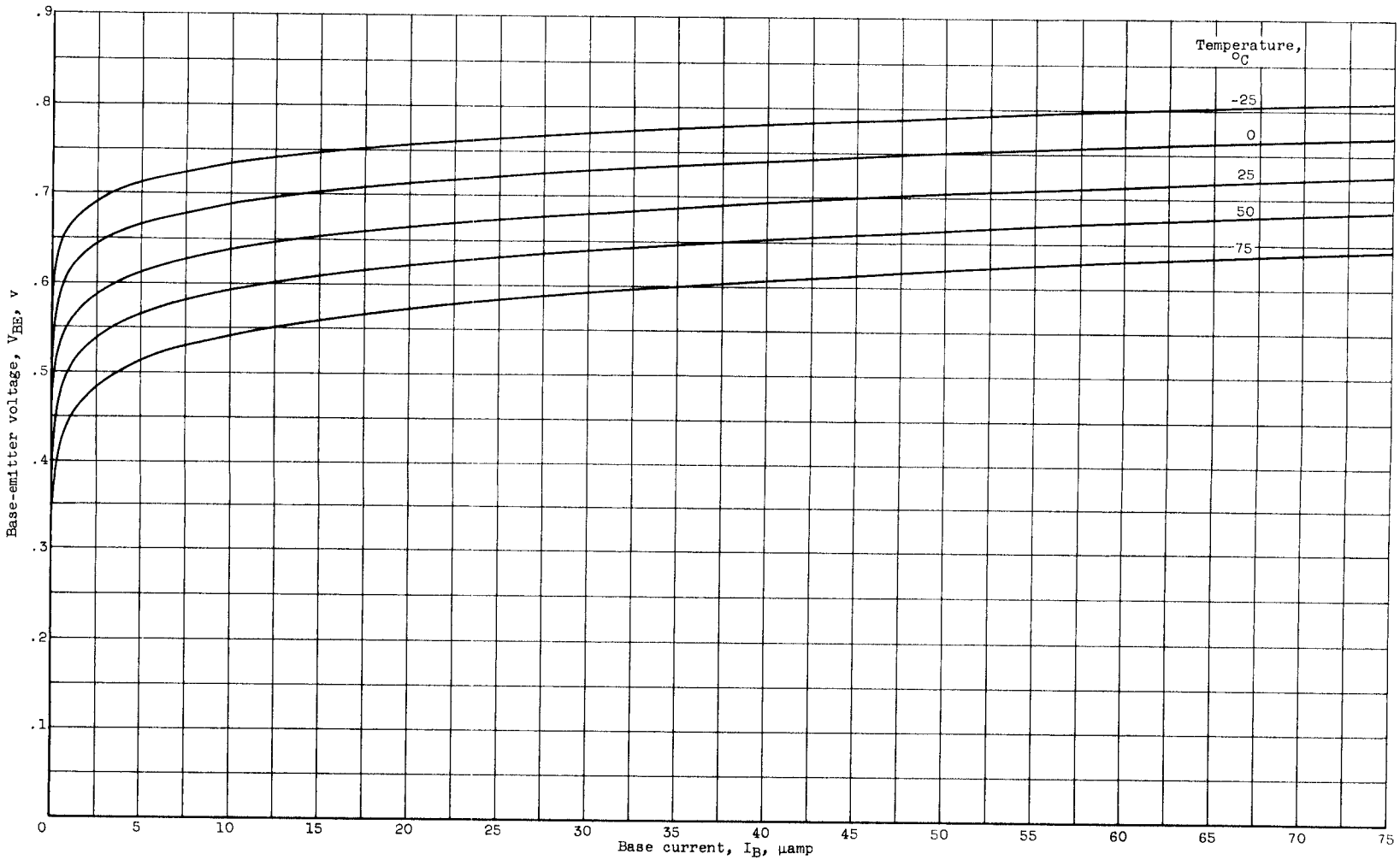
(b) NPN transistor. Collector-emitter voltage, 1.5 volts.

Figure 10. - Direct-current gain as function of collector current.



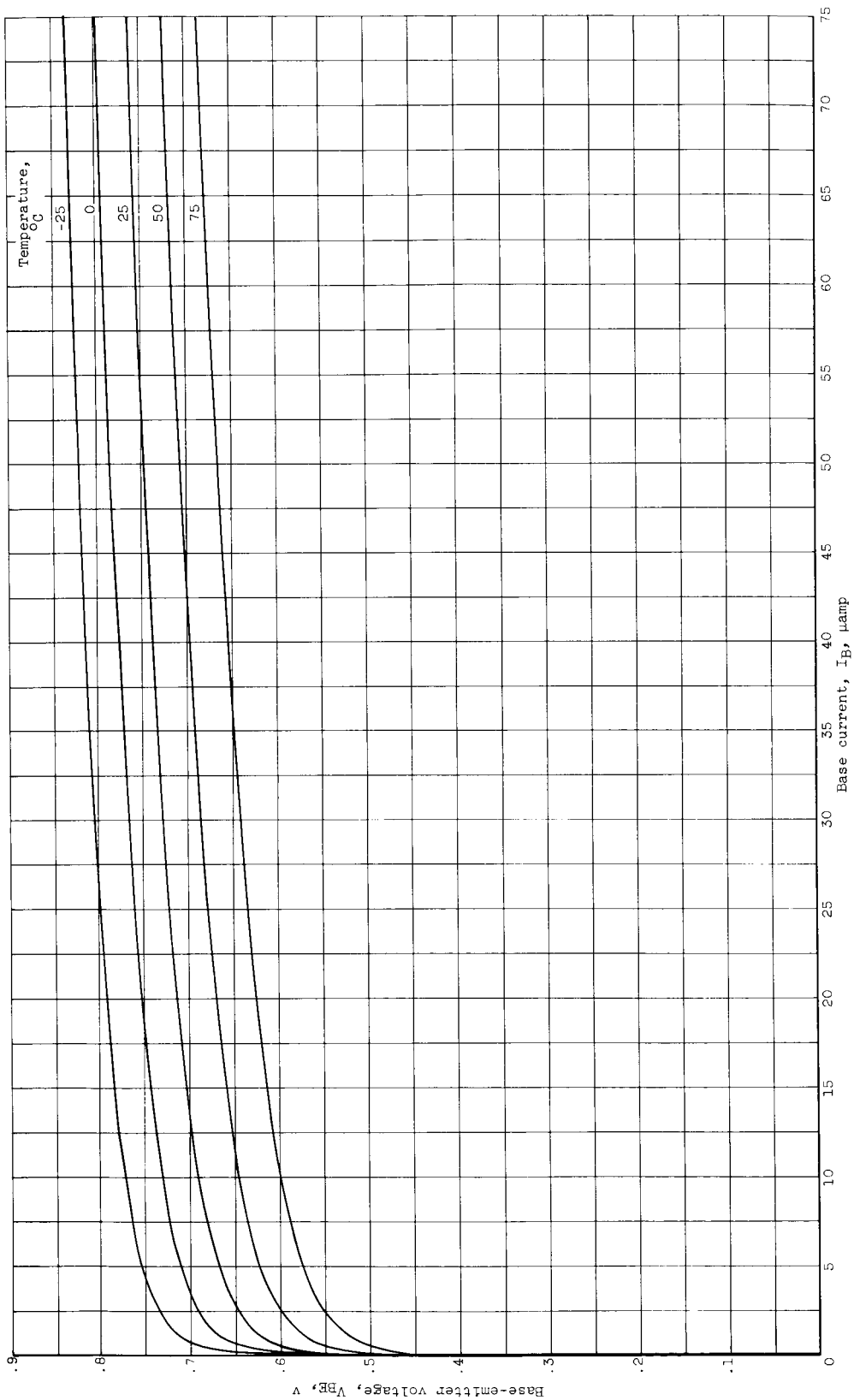
(a) Type 2N2432 (NPN).

Figure 11. - Typical base-emitter voltage characteristics of silicon transistor.



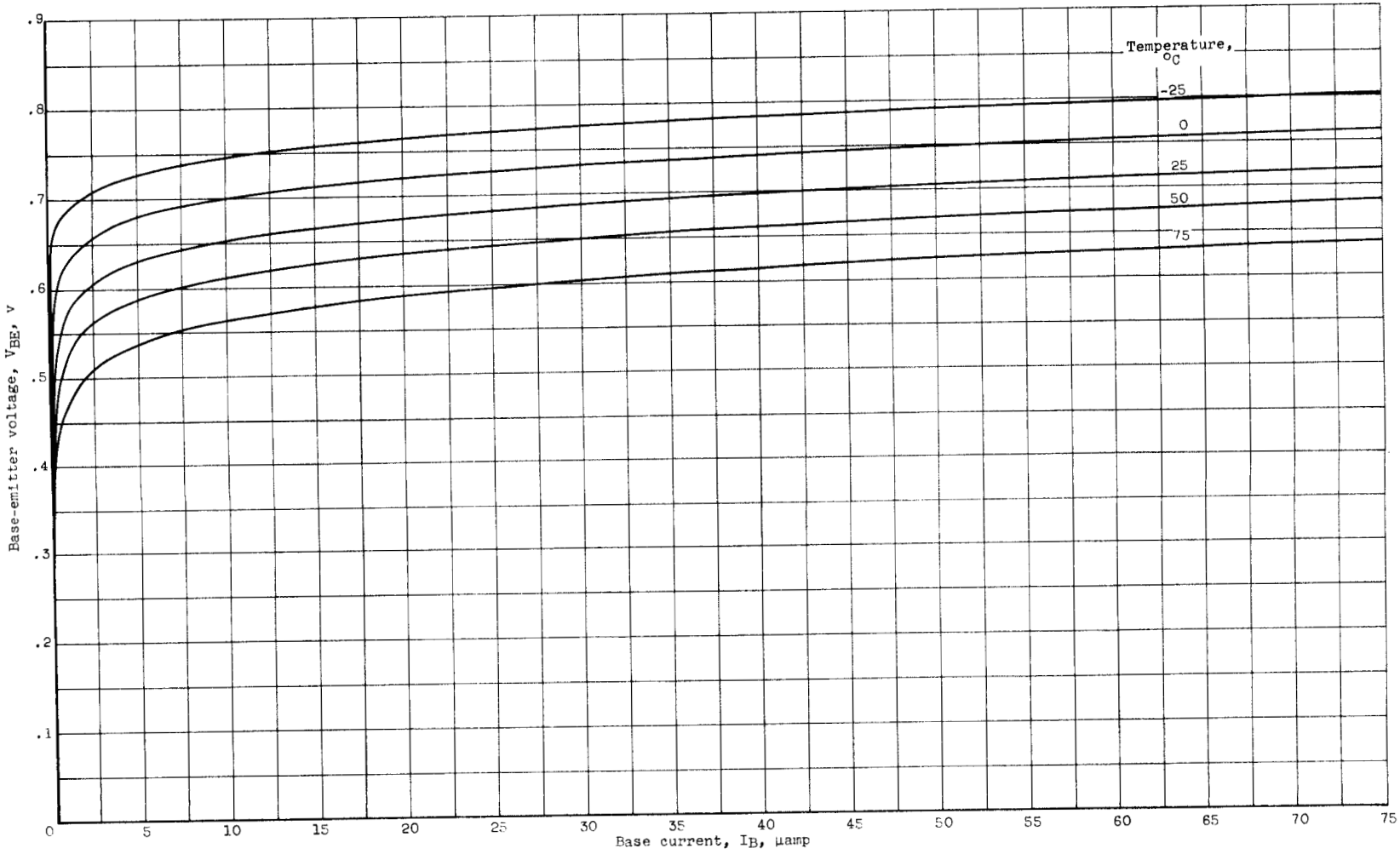
(b) Type HA9038 (PNP).

Figure 11. - Continued. Typical characteristics of silicon transistor.



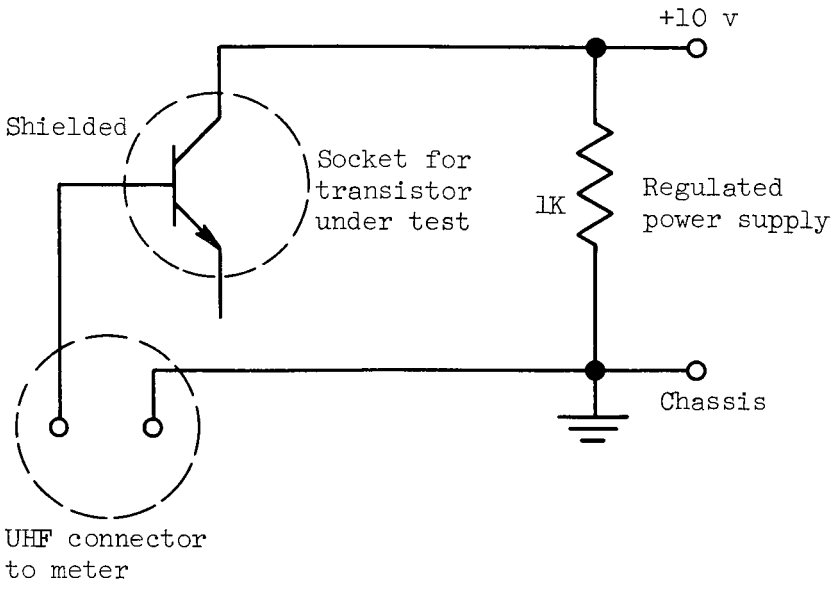
(c) Type 2N2412 (PNP).

Figure 11. - Continued. Typical base-emitter voltage characteristics of silicon transistor.

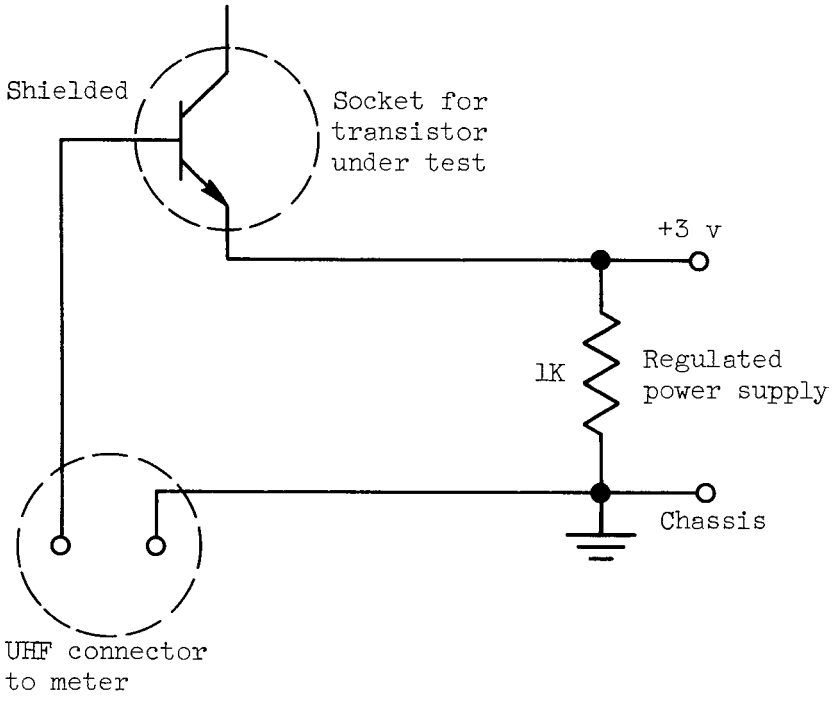


(d) Type 2N930 (NPN).

Figure 11. - Concluded. Typical base-emitter voltage characteristics of silicon transistor.

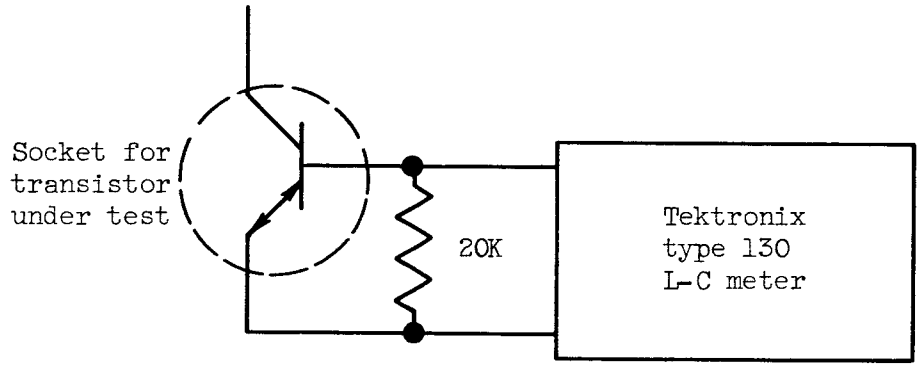


(a) Collector-base leakage current.

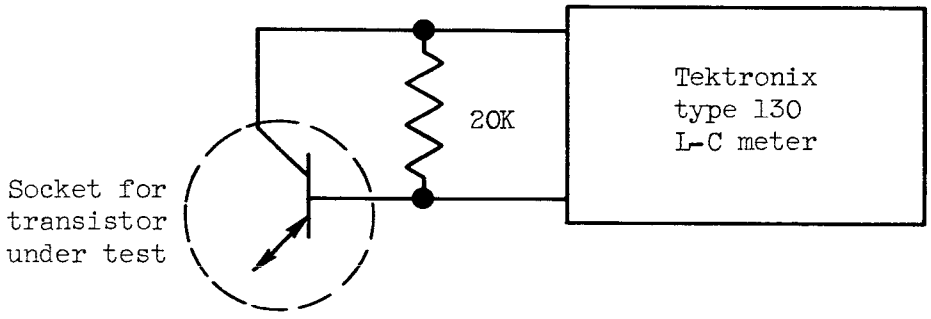


(b) Emitter-base leakage current.

Figure 12. - Circuits for measuring leakage currents for Keithley instrument model 610A electrometer.



(a) Input capacitance.



(b) Output capacitance.

Figure 13. - Capacitance measurements. The 20K shunting resistor reduces voltage impressed across junction to approximately 0.3-volt alternating-current peak-to-peak voltage. (Without resistor, 1.1-volt alternating-current peak-to-peak voltage.)